Curriculum Vitae

Avinoam Kolodny

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Personal Data:

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Academic Degrees:

1975   D.Sc.   Department of Electrical Engineering, Technion.

1977   M.Sc.   Department of Electrical Engineering, Technion (Cum Laude).

1980   D.Sc.   Department of Electrical Engineering, Technion (Summa Cum Laude).

Academic Appointments:

2016-present   Professor, Department of Electrical Engineering, Technion.

2010–2015   Associate Professor, Department of Electrical Engineering, Technion.

2006–2009   Senior Lecturer, Department of Electrical Engineering, Technion.

2000–2006   Senior Research Associate, Department of Electrical Engineering, Technion.

1999   Visiting Scientist, Department of Electrical Engineering, Technion.

1984–1999   Adjunct Senior Lecturer, Technion.

1980–1981   Lecturer, Department of Electrical Engineering, Technion.

1974–1979   Teaching Assistant/Instructor, Technion.

Professional Experience:

1999–present   Faculty Member, Department of Electrical Engineering, Technion.
               Initiated research in VLSI Interconnect Architecture,
               Networks-on-Chips, Multi-Core Processors and Memristive Circuits.
               Head of the EE Undergraduate Studies Committee.
               Co-director of the Advanced Circuit Research Center.

1992–1999   Manager of Training and Capability Development at Intel, Israel.
               Contributed to people development and organizational learning processes in
               Intel's Israel operations, including technical courses, management
               development, project planning and tracking, and organizational development.

1988–1992   R&D Manager in charge of Intel's Performance Verification tools (timing
               analysis, logic synthesis) in Haifa, Israel. Led development of Intel's in-house

CAD tool system for ensuring the internal timing performance of Pentium microprocessors.

1986–1988   Manager of Intel's Corporate CAD system architecture in Santa Clara, California. Architected one of the first industrial-strength VLSI CAD systems using a hardware-description language, logic synthesis tools adapted directly from academic research, novel static path analysis, electrical rule-checking, and VLSI layout tools. Coordinated Intel's liaison with ongoing research at U.C. Berkeley in electronic CAD.

1983–1986   Team leader of schematic logic verification and circuit debugging CAD tools at Intel, Israel. Received Intel's Individual Achievement Award for developing software, which later became the foundation for multiple integrated capabilities within Intel's CAD system.

1983   Director of Technology and CAD at the start-up of Zoran Corporation in Sunnyvale, CA. Managed the research of a new anti-fuse memory.

1981–1983   Device physicist in the Advanced Devices group of Non-Volatile Memory Technology Development (EPROM, EEPROM) at Intel Corp., Santa Clara, CA. Conducted research on thin dielectrics and floating-gate memory devices in silicon. Contributed to the development of the "hybrid memory cell", which evolved into commercial Flash memory.

1980–1981   Participated in development and evaluation of Silicon MOS and CCD integrated circuit processing at the Technion.

1975–1980   Research towards M.Sc. and D.Sc. in physics and technology of narrow-bandgap semicondutor devices for infrared detector applications. Implemented and investigated electronic devices in Indium Antimonide and Mercury-Cadmium-Telluride. Reported the first MOS transistors in Mercury-Cadmium-Telluride; interpreted and modeled two-dimensional effects in infrared photodiodes and photoconductors.

Research Interests:

Electronic design automation; Device, circuit and system modeling; Low power design; Engineering methodologies; VLSI architecture; VLSI interconnect; Networks on Chips; Multi-core processor systems, Memristor-based circuits and systems.

Teaching Experience:

Undergraduate courses:

"Basics of Semiconductor Devices"
"Integrated Circuits and VLSI design"
"Linear Circuits"
"Switching Circuits"
"Microprocessors"
"Electronic Devices 1 (MOS)".

Graduate courses:

"Modeling and Optimization of VLSI Interconnect"
"CAD of VLSI Systems"
"MOS Device Modeling"
"VLSI Architectures"
"Managers Development in High-Tech Industries"
(Faculty of Industrial Engineering & Management; developed in 1996).

Professional Activities:

2003–2012 Associate Editor, Journal of Circuits, Systems and Computers.

2006–Present Member of the Systems and Applications Technical Committee (VSA-TC) of the IEEE Circuits and Systems Society (IEEE-CASS).

2006–2007 R&D Manager in charge of Intel's Performance Verification tools (timing analysis, logic synthesis) in Haifa, Israel. Led development of Intel's in-house CAD tool system for ensuring the internal timing performance of Pentium microprocessors.

2006–2007 Program committee co-chairman, IEEE 1st International Symposium on Networks on Chips, Princeton University, May 2007.

2008 Guest co-editor of IEEE Transactions on VLSI systems, special issue on Networks on Chips.

2008 ACM/IEEE System Level Interconnect Prediction workshop (SLIP) program committee member, special sessions chair.

16th International Conference on VLSI-SoC program committee member.

NOCS 2008 Technical Program Committee member.

2009 Technical Program Committee member for NOCS 2009, DATE 2009.

2010–2015 Technical Program Committee member for NOCS conference.

Technion Activities:

2012–2013 Member of Technion Committee to Assess the Structure and Load of Undergraduate Studies ("Vaadat Omes" headed by Prof. Yachin Cohen).

2012–2013 Member of the Steering Committee of "Future Scientists" program.

2013–Present Member of preparatory for the department of arts and humanities.

2017 Member of Technion Committee to revise course teaching survey.

Departmental Activities:

2007–Present Head of the Undergraduate Studies Committee in the EE Dept.

2008-Present Co-director of Advanced Circuits Research Center (ACRC)

Honors:

1986   Intel Individual Achievement Award in recognition of outstanding contribution.

2000-present: Received more than 12 Technion Awards for excellence in teaching.

2001   Jacknow Award for Excellence in Teaching, Technion Board of Governors.

2003   Fulbright Alumni Initiative Awards program, "Joint Research-Oriented graduate course in Advanced VLSI Circuits and Systems" (in collaboration with Prof. Eby G. Friedman, University of Rochester, NY).

2005   GLSVLSI Best Student Paper Award: M. Popovich, E. G. Friedman, M. Sotman, and A. Kolodny, "On-Chip Power Distribution Grids with Multiple Supply Voltages for High Performance Integrated Circuits," Proceedings of the ACM Great Lakes Symposium on VLSI, pp. 2–7, April 2005.

2007   Salomon Simon Mani Award for Excellence in Teaching, Technion Board of Governors.

2008   SPAA Best Paper Award: Z. Guz, I. Keidar, A. Kolodny, and U. Weiser, "Utilizing Shared Data in Chip Multiprocessors with the Nahalal Architecture," 20th ACM Symp. on Parallelism in Algorithms and Architectures (SPAA'08), special track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines, June 2008.

2009   Dudi Ben-Aharon Research Prize, awarded by the Technion's VP of research; "Utilizing Shared Data in Chip Multiprocessors with the Nahalal Architecture" (jointly with Idit Keidar).

2011   Yannai Prize for Excellence in Academic Education, Technion.

2012   EEE Circuits and Systems Society, VLSI Transactions Best Paper Award: A. Morgenshtein, E. G. Friedman, R. Ginosar and A. Kolodny, "Unified Logical Effort - A Method for Delay Evaluation and Minimization in Logic Paths with RC Interconnect," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 18, No. 5, pp. 689-696, May 2010.

2013   Sanford Kaplan prize awarded by Bronica Entrepreneurship Center, Technion, for the venture "Design Solutions and Methodologies for Enhancing CMOS VLSI with Emerging Memory Technologies" (jointly with Shahar Kvatinsky, Eby Friedman, and Uri Weiser).

2014   Hershel Rich Technion Innovation Award; "Multistate Registers and Continuous Flow Multithreading" (jointly with Shahar Kvatinsky, Eby Friedman, and Uri Weiser).

2015   IEEE Circuits and Systems Society, Guillemin-Cauer Award (Best Paper published in Transactions on Circuits and Systems): S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM – ThrEshold Adaptive Memristor Model," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 60, No. 1, pp. 211-221, January 2013.

2016   Fellow of the IEEE, for contributions to VLSI design and automation tools.

Graduate Students:
D.Sc.

1. Evgeny Bolotin, "Network On Chip",
   with I. Cidon (principal supervisor after conversion to direct PhD track) and R. Ginosar.
   Graduated: 2007; Currently with Nvidia, CA.

2. Arkadiy Morgenshtein, "Links for Network-on-Chip",
   (with E. Friedman and R. Ginosar (principal supervisor)
   Graduated: 2008; Currently with IBM.

3. Konstantin Moiseev, "CMOS layout migration automation", (principal supervisor, with S. Wimer).
   Graduated: 2010 currently with Intel.

4. Reuven Dobkin, "High speed asynchronous communication for SoC",
   (with R. Ginosar (principal supervisor)). *Graduated: 2009.*

5. Zigi Walter, "Network on Chip for CMP", (with I. Cidon (principal supervisor)).
   Graduated: 2010 currently with Intel.

6. Zvika Guz ,"Cache organization for chip multiprocessor",
   (with U. Weiser (principal supervisor) and I. Keidar).
   Graduated: 2010, currently with Nvidia, CA.

7. Ran Manevich, "Bus enhanced Network on Chip",
   (principal supervisor, with I. Cidon.)
   Graduated: 2014, currently with IDF.

8. Yaniv Ben-Izhak, (principal supervisor, with I. Cidon).
   Graduated: 2014, currently with IBM.

9. Shahar Kvatinsky, "Memristor-based circuits and architectures",
   (principal supervisor, with E. Friedman and U. Weiser).
   Graduated: 2014, currently an assistant professor at Technion.

10. Tomer Morad, "Asymmetric Clustered Chip Multiprocessors",
    (principal supervisor, with U. Weiser).
    Graduated: 2016, currently a post-doc at ConellTech.

11. Eitan Zahavi, "Lossless networks in and out of the chip",
    (principal supervisor, with I. Keslassy and I.Cidon).
    Graduated: 2016, currently with Mellanox.

M.Sc.

1. Yaron Elboim, "Clocking issues in System-On-Chip design", (with D. Ginosar).
   Graduated: 2001; Currently with Wilocity.

2. Noam Dolev, "Integrated low-voltage delta-sigma conversion circuits in digital CMOS Technology".
   Graduated: 2002; Currently a Ph.D. student at Stanford University.

3. Oleg Milter, "Synthesis of CMOS VLSI circuits considering digital noise effects".
   Graduated: 2002; Currently logic synthesis team leader in the mobile processors division at Intel.

4. Georgy Schupak, "High-speed, low-power medium-size cache design".
   Graduated: 2002; Currently design team leader at Intel's mobile processors division.

5. Oleg Kosyakovsky, "Approaches to managing Trace Cache in computer systems",

(With A. Mendelson (principal supervisor)).
Graduated: 2002; Currently a software engineer at Intel.

6. Nir Magen, "Power Issues in VLSI Interconnect", (Principal supervisor, with U. Weiser.
Graduated: 2003; Joined Intel after graduation. Died in a road accident in 2005.

7. Assad Khamaisee, "Combining trace cache and value prediction", (with A. Mendelson principal supervisor).
Graduated: 2003; Currently with Mellanox.

8. Michael Moreinis, "Repeater insertion in deep submicron VLSI circuits".
Graduated: 2004; Currently a circuit designer at Intel.

9. Tomer Morad, "Data trace cache", (with Dr. U. Weiser (principal supervisor)).
Graduated: 2005; Currently with Horizon semiconductor and a PhD student.

10. Shay Michaely, "Wiring modifications for optimal migration of processors", 2005.
(with S. Wimer). *Graduated: 2005.*

11. Konstantin Moiseev, "Performance optimization by wire reordering", (with S. Wimer).
Graduated: 2005; Currently with Intel.

12. Walter Isaskhar, "Functional interfaces for Network-On-Chip", (with I. Cidon (principal supervisor) and R. Ginosar).
Graduated: 2005; Currently with Intel.

13. Michael Behar, "Hot traces in modern processors", (with A. Mendelson (principal supervisor)).
Graduated: 2005; Currently with Intel.

14. Anastasia Barger, "Modeling and design of Network-on-Chip interconnects".
Graduated: 2006; Currently with Intel.

15. Michael Sotman, "Power delivery structures in VLSI".
Graduated: 2006; Currently with Intel.

16. Dror Barash, "Cache Manipulations to Improve Multimedia Applications", (with U. Weiser (principal supervisor)).
Graduated: 2007.

17. Iris Sorani, "Long Instruction Traces and their Usage", (with A. Mendelson (principal supervisor)).
Graduated: 2007; currently with Intel.

18. Evgeny Krimer, "Evaluation and Optimization of Transmission Latencies in a Network-On-Chip", (with Dr. I. Kelassy (principal supervisor)).

Graduated: 2009; currently a PhD student at UT Austin.

19. Chen Damishian, "Improving cache management policy by identifying repeated sequences of accesses", (with Dr. A. Mendelson (principal supervisor)).
Graduated: 2009; currently with Intel.

20. Yaniv Ben-Izhak, "Performance and Power Aware Threads Allocation for NoC CMP", (with I. Cidon (principal supervisor)).
Graduated: 2009. Currently a PhD student.

21. Inna Vaisband, "Low Power Clocking," (with E. Friedman and R. Ginosar (principal supervisor)). *Graduated: 2009; currently a PhD student at U. Rochester.*

22. Yoni Aizik, "Design Considerations for Low Power CMOS Digital Circuits".
Graduated: 2009; currently with Intel.

23. Shmuel Zobel, "Performance-power tradeoffs in General Purpose Graphics Processors," (with A. Mendelson (principal supervisor)).
    Graduated: 2010; currently with Intel.

24. Ameer Abdel-Hadi, "Non-uniform Mesh clocking," (with E. Friedman and R. Ginosar).
    Graduated: 2010; currently a PhD student at UBC.

25. Anna Kouslik, "Power Macro-modeling in VLSI design",
    Graduated: 2010; currently with Intel.

26. Gregory Sizikov, "Design and Analysis of Integrated Voltage Regulators",
    (with E. Friedman). *Graduated: 2011; currently with Google.*

27. Yaron Cohen, "Low Power D/A Converter Design Considerations", (with R. Ginosar (principal supervisor)).
    Graduated: 2012; currently with CSR.

28. Victoria Vishnyakov, "Inductive effects in on-chip interconnect", (with E. Friedman).
    Graduated: 2012; currently with Intel.

29. Amnon Stanislavsky, "Power-driven floorplanning", (with S. Wimer).
    Graduated: 2013; currently with Intel.

30. Roman Malits, "Novel thread scheduling in GPGPU",
    (with A. Mendelson (principal supervisor)).
    Graduated: 2012; currently with Rafael.

31. Leon Polishuk, "Latency considerations for NoC interconnection fabrics" (with I. Cidon).
    Graduated: 2013; currently with Intel.

32. Yifat Levy, "Digital circuits design using memristors" (with E. Friedman).
    Graduated: 2014; currently with Intel.

33. Loren Jammal, "Avoiding memory-storage bottlenecks" (with U. Weiser).

Research Grants:

2001 - Intel Corp., $100,000, On-chip and off-chip interconnect. (Kolodny, Werner).

2003 - Intel Corp., $10,000, Networks on Chip. (Cidon, Ginosar, Kolodny).

2004 - ISRC, IS 450,000, Network on Chip (Cidon, Ginosar, Kolodny).

2004 - "SRC, $180,000, Power and Area Efficient Network-on-Chip Architectures (Semiconductor Research Corporation, USA) (Cidon, Ginosar, Kolodny).

2004   Intel Corp., $10,000, Power Delivery structures in CMOS VLSI (Kolodny).

2004 - Intel Corp., $80,000, Interconnected Multi-Core Processor Architecture (Cidon, Ginosar, Keidar, Kolodny).

2005 - Intel Corp. $80,000, Interconnected Multi-Core Processor Architecture − extension (Cidon, Ginosar, Keidar, Kolodny).

2005 - Intel Corp., $10,000, Power Delivery structures in CMOS VLSI – extension (Kolodny).

2006 - Intel Corp., $80,000, Interconnected Multi-Core Processor Architecture − extension (Cidon, Ginosar, Keidar, Kolodny).

2006 - Intel Corp., $12,000, Power modeling and power delivery structures in CMOS VLSI.

2007 - Freescale Corp., $20,000, Network-on-Chip for CMP (Cidon, Ginosar, Kolodny).

2007 - Israel Ministry of Industry and Commerce, ALPHA consortium, IS 127,584, Automatic insertion of power management circuits (Kolodny).

2007 - Intel Corp., $12,000, Power modeling (extension) (Kolodny).

2007 - Intel Corp., $80,000, Interconnected Multi-Core Processor Architecture − extension (Cidon, Ginosar, Keidar, Kolodny, Weiser).

2008 - ACRC yearly grant of $300,000 by five companies (Ginosar, Kolodny, Ritter).

2008 - SRC, $60,000 per year for 3 years, Multi-Core Cache Architectures (Ginosar, Keidar, Kolodny, Weiser).

2008 - Intel Corp., $12,000, Power modeling (extension) (Kolodny).

2009 - Israel Ministry of Industry and Commerce, ALPHA consortium, IS 136,080

2009 - Intel Corp., $72,000, Interconnected Multi-Core Processor Architecture − extension (Cidon, Ginosar, Keidar, Kolodny, Weiser).

2010 - Israel Ministry of Industry and Commerce, ALPHA consortium.

2010 - Intel Corp. $150,000, Heterogeneous Computing the Inevitable solution: Power Management, Scheduling and ISA (Cidon, Ginosar, Keslassy, Keidar, Kolodny, Weiser)

2012 - Member of Intel Collaborative Research Institute for Computational Intelligence

2013 - U.S.-Israel Binational Science Foundation (BSF) - $110,000 Computing Structures Beyond Moore and von Neumann (Friedman, Kolodny, Weiser)

2015 - Intel Corp. $150,000, Memory Intensive Architectures (Friedman, Kolodny, Kvatinsky, Weiser)

Publications:

Theses:

J1   A. Kolodny, Phototransistor in Indium Antimonide, M.Sc. thesis, Technion - I.I.T., 1977 . Supervisor: Prof. Joseph Shappir.

J2   A. Kolodny, Electro-optical Properties of Electron Devices in Mercury-Cadmium Telluride, D.Sc. thesis, Technion - I.I.T., 1980. Supervisor: Prof. Itzhak Kidron.

Refereed papers in professional journals

J3   J. Shappir and A. Kolodny, "The Response of Small Photovoltaic Detectors to Uniform Radiation," IEEE Transactions on Electron Devices, Vol. ED-24, pp.1093-1098, 1977.

J4   T. Bernstein and A. Kolodny, "A Useful Method for Approximating the Profile of Ions Implanted through a Thin Film," IEEE Trans. on Electron Devices, Vol. ED-24, pp.1365-1366, 1977.

J5   A. Kolodny and J. Shappir, "Diffusion Properties of Cadmium in InSb," Journal of the Electrochemical Society, Vol.125, no. 9, pp.1530-1534, 1978.

J6   A. Kolodny, "Current Gain of Shallow-Junction Lateral Transistors," IEEE Transactions on Electron Devices, Vol. ED-26, pp.987-989, 1979.

J7   A. Kolodny and I. Kidron, "Properties of Ion-Implanted Junctions in Mercury-Cadmium-Telluride," IEEE Transactions on Electron Devices, Vol. ED-27, pp.37-43, 1980.

J8   A. Kolodny, Y.J. Shacham-Diamand and I. Kidron, "N-Channel MOS Transistors in Mercury-Cadmium-Telluride," IEEE Transactions on Electron Devices, Vol. ED-27, pp.591-595, 1980.

J9   J. Shappir, A. Kolodny and Y.J. Shacham-Diamand, "Diffusion Profiling Using the Graded C-V Method," IEEE Transactions on Electron Devices, Vol. ED-27, p.993, 1980.

J10   D. Lubzens, A. Kolodny and Y. Shacham, "Automated Measurement and Analysis of MIS Interfaces in Narrow-Bandgap Semiconductors," IEEE Transactions on Electron Devices, Volume 28, Issue 5, pp. 546 – 551, 1981.

J11   A. Kolodny and I. Kidron, "Two-dimensional Effects in Intrinsinc Photo-Conductive Infrared Detectors," Infrared Physics, Vol. 22, pp.9-22, 1982.
*(This paper has been selected for reprint also in Infrared Design (SPIE Volume 513), edited by R.B. Johnson and W.L. Wolfe, 1983.)

J12   B. Eitan and A. Kolodny, "Two Components of Tunneling Current in MOS Structures," Applied Physics Letters, Vol. 43, pp.106-108, 1983.

J13   A. Kolodny, S. Nieh, B. Eitan and J. Shappir, "Analysis and Modeling of Floating-gate EEPROM Cells," IEEE Transactions on Electron Devices, Volume 33, Issue 6, pp. 835 – 844, 1986.
* (This paper has been selected for reprint also in Nonvolatile Semiconductor Memories, edited by Chenming Hu, IEEE Press Selected Reprint Series, New York, 1991, pp. 128-137.)

J14   Y. Elboim, R. Ginosar and A. Kolodny, "A Clock Tuning Circuit for System on Chip," IEEE Transactions on VLSI, vol. 11, pp.616-626, 2002.

J15   O. Milter and A. Kolodny, "Crosstalk Noise Reduction in Synthesized Digital Logic Circuits," IEEE Transactions on VLSI , Volume: 11, pp. 1153 - 1158, Dec. 2003.

J16   E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny, "QNoC: QoS architecture and design process for cost-effective Network on Chip," Special issue on Networks on Chip, The Journal of Systems Architecture, Volume 50, pp. 105-128, February 2004.

J17   E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny , "Cost considerations in Network on Chip" , Special issue on Networks on Chip, Integration - the VLSI journal, Vol. 38, No. 1, pp. 19-42, Oct. 2004.

J18   N. Dolev, A. Kornfeld and A. Kolodny, "Comparison of Sigma-Delta Converter Circuit Architectures in Digital CMOS Technology," Journal of Circuits, Systems and Computers, vol. 14, No. 3, pp.1-18, 2005.

J19   T. Morad, U. Weiser, A. Kolodny, M. Valero and E. Ayguade, "Performance, Power Efficiency and Scalability of Asymmetric Cluster Chip Multiprocessors," IEEE Computer Architecture Letters, vol. 4, 2005.

J20   S. Wimer, S. Michaely, K. Moiseev and A. Kolodny, "Optimal Bus Sizing in Migration of Processor Design," IEEE Transactions on Circuits and Systems I: Regular Papers, Fundamental Theory and Applications, Volume 53, Issue 5, pp. 1089 – 1100, May 2006.

J21   M. Moreinis, A. Morgenshtein, I. Wagner and A. Kolodny, "Logic gates as Repeaters," IEEE Transactions on VLSI , Volume 14, pp.1276 - 1281, Nov. 2006.

J22   M. Behar, A. Mendelson and A. Kolodny, "Trace Cache Sampling Filter," ACM Transactions on Computer Systems 25, 1 (Feb. 2007), 3, pp.1-32.

J23   Z. Guz, I. Walter, E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny, "Network Delays and Link Capacities in Application-Specific Wormhole NoCs," VLSI Design - Special issue on Networks on Chip, Volume 2007 (2007), Article 90941.

J24   Z. Guz, I. Keidar, A. Kolodny and U. C. Weiser, "Nahalal: Memory Organization for Chip Multiprocessors", IEEE Computer architecture letters, Vol. 6, No. 1, June 2007.

J25   K. Moiseev, S. Wimer and A. Kolodny, "On optimal ordering of signals in parallel wire bundles," Integration – the VLSI Journal, Vol. 41, 2008, pp. 253 – 268.

J26   M. Popovich, M. Sotman, A. Kolodny and E. G. Friedman, "Effective Radii of On-Chip Decoupling Capacitors," IEEE Transactions on Very Large Scale Integration (VLSI) Systems , Vol. 16, No. 7, pp.894-907, July 2008.

J27   M. Popovich, E. G. Friedman, M. Sotman and A. Kolodny, "On-Chip Power Distribution Grids with Multiple Supply Voltages for High Performance Integrated Circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 7, pp.908-921, July 2008.

J28   I. Walter, I. Cidon, and A. Kolodny, "BENoC - A Bus-Enhanced Network on-Chip for a Power Efficient CMP", IEEE Computer Architecture Letters, Volume 7, Issue 1, 2008.

J29   K. Moiseev, A. Kolodny and S. Wimer, "Timing-Aware Power-Optimal Ordering of Signals," ACM Transactions on Design Automation of Electronic Systems, Vol. 13, No. 4, Article 65, Sept. 2008.

J30   R. Dobkin, R. Ginosar, A. Kolodny, "QNoC Asynchronous Router," Integration , the VLSI Journal, Vol. 42, pp.103-115, February 2009.

J31   K. Moiseev, A. Kolodny and S. Wimer, "Power-Delay Optimization in VLSI
        Microprocessors by Wire Spacing," ACM Transactions on Design Automation of
        Electronic Systems (TODAES), Volume 14, Issue 4 (August 2009), Article No. 55,
        2009, ISSN: 1084-4309.

J32   Z. Guz, E. Bolotin, I. Keidar, A. Kolodny, A. Mendelson and U. Weiser, Many-Core
        vs. Many-Thread Machines: Stay Away From the Valley", IEEE Computer
        Architecture Letters, Volume 8, Issue 1, Jan. 2009.

J33   A. Morgenshtein, E. G. Friedman, R. Ginosar and A. Kolodny, "Unified Logical
        Effort - A Method for Delay Evaluation and Minimization in Logic Paths with RC
        Interconnect," IEEE Transactions on Very Large Scale Integration (VLSI) Systems,
        Vol. 18, No. 5, pp. 689-696, May 2010.
        (IEEE Circuits and Systems Society Transactions best paper award 2012).

J34   R. Dobkin, R. Ginosar, A. Kolodny and M. Moyal, "Asynchronous Current Mode
        Serial Communication," Very Large Scale Integration (VLSI) Systems, IEEE
        Transactions on , vol.18, no.7, pp.1107-1117, July 2010.

J35   K. Moiseev, A. Kolodny and S. Wimer, "Interconnect Bundle Sizing under Discrete
        Design Rules", Computer-Aided Design of Integrated Circuits and Systems, IEEE
        Transactions on , vol.29, no.10, pp.1650-1654, Oct. 2010.

J36   E. Krimer, M. Erez, I. Keslassy, A. Kolodny and I. Walter, "Static Timing Analysis
        for Modeling QoS in Networks on Chip", Journal of Parallel and Distributed
        Computing (5): 687-699 (2011).

J37   I. Vaisband, E. G. Friedman, R. Ginosar and A. Kolodny, "Low Power Clock
        Network Design," J. Low Power Electron. Appl., 1(1), 219-246, 2011.

J38   R. Manevich, I. Cidon, A. Kolodny, and W. Isask'har, "Centralized Adaptive Routing
        for NoCs," Computer Architecture Letters , vol.9, no.2, pp.57-60, Feb. 2010.

J39   S. Wimer, K. Moiseev and A. Kolodny, "On VLSI Interconnect Optimization and
        Linear Ordering Problem", Optimization and Engineering, Volume 12, Issue 4, pp.
        603-609, 2011.

J40   Y. Aizik and A. Kolodny, "Finding the Energy Efficient Curve: Gate Sizing for
        Minimum Power under Delay Constraints," VLSI Design, 2011.

J41   Evgeni Krimer, Isaac Keslassy, Avinoam Kolodny, Isask'har Walter, Mattan Erez,
        "Static timing analysis for modeling QoS in networks-on-chip," J. Parallel Distrib.
        Comput. 71(5): 687-699 (2011).

J42   T.Y. Morad, A. Kolodny and U.C. Weiser, "Task Scheduling Based On Thread
        Essence and Resource Limitations," Journal of Computers, Vol. 7, Issue 1, 2012.

J43   K. Moiseev, A. Kolodny and S. Wimer, "The complexity of VLSI power-delay
        optimization by interconnect resizing," Journal of Combinatorial Optimization,
        Volume 23, Issue 2 (2012), pp. 292-300.

J44   V. Vishnyakov, E.G. Friedman and A. Kolodny, "Multi-Aggressor Capacitive and
        Inductive Coupling Noise - Modeling and Mitigation", Microelectronics Journal
        Vol. 43 (2012), pp. 235-243.

J45   R. Malits, E. Bolotin, A. Kolodny and A. Mendelson, "Exploring the Limits of
        GPGPU Scheduling," ACM Transactions on Architecture and Code Optimization
        (TACO) 8(4): 29 (2012).

J46   E. Zahavi, I. Cidon and A. Kolodny, "GANA: A Novel Low Cost Conflict Free NoC Architecture," ACM Transactions on Embedded computing systems 12(4): 109 (2013).

J47   A. Abdelhadi, R. Ginosar, A. Kolodny, E. G. Friedman, "Timing–driven variation– aware synthesis of hybrid mesh/tree clock distribution networks," Integration, the VLSI Journal, Volume 46, Issue 4, Pages 382-391, September 2013.

J48   S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM -ThrEshold Adaptive Memristor Model," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 60, No. 1, pp. 211-221, January 2013.

J49   E. Zahavi, I. Keslassy and A. Kolodny, "Distributed| Adaptive Routing Convergence to Non-Blocking Data Center Network Routing Assignments", IEEE Journal on Selected Areas in Communications 32(1): 88-101 (2014).

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J58   D. Soudry, D. Di Castro, A. Gal, A. Kolodny, and S. Kvatinsky, "Memristor-Based Multilayer Neural Networks With Online Gradient Descent Training," accepted to IEEE Transactions on Neural Networks and Learning (TNNLS), vol. 26, pp. 2408-2421, 2015.

J59   S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "VTEAM – A General Model for Voltage Controlled Memristor," Transactions on Circuits and Systems II: Express Briefs, volume 62, August 2015, pp. 786-790.

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J61   R. Manevich, I. Cidon, A. Kolodny, "Design and Dynamic Management of Hierarchical NoCs", accepted to Microprocessors and Microsystems, vol. 40, pp. 154-166, 2016.

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C2   A. Kolodny, R. Friedman and T. Ben-Tzur, "Rule-based Static Debugger and Simulation Compiler for VLSI Schematics," Proceedings of 1985 IEEE International Conference on Computer-Aided Design (ICCAD), Santa Clara, CA, Nov. 1985.

C3   Y. Elboim, A. Kolodny, R. Ginosar, "A Clock Tuning Circuit for IP Core Integration in SoC," International workshop on IP-based synthesis and SoC design, Grenoble, France, Dec. 2000.

C4   Y. Elboim, A. Kolodny, R. Ginosar, "A Clock Tuning Circuit for IP Core Integration in SoC," Proc. DesigCon 2001, January 2001, Santa Clara, CA.

C5   O. Kosyakovsky, A. Mendelson and A. Kolodny,. "The use of profile-based trace classification for improving the power and performance of trace cache systems," 4th Workshop on Feedback-Directed and Dynamic Optimization (FDDO-4), Austin, Texas, December 2001.

C6   Y. Elboim, R. Ginosar and A. Kolodny, "A Clock Tuning circuit for System on Chip," ACiD-WG 2002 Workshop, Munich, Germany, January 2002.

C7   O. Milter and A. Kolodny, "Crosstalk Delay Analysis and Prevention Using PrimeTime SI and Design Compiler in High Frequency CPU Design," Proc. SNUG, Boston, Mass., September 2002.

C8   Y. Elboim, R. Ginosar and A. Kolodny, "A Clock Tuning Circuit for System on Chip," Proceedings of ESSCIRC 2002, Florence, Italy, September 2002.

C9   A. Khamaisee, A. Mendelson and A. Kolodny, "Can hot traces help value prediction?," 1st Value-prediction workshop, San Diego, CA, June 2003.

C10   A. Morgenshtein, M. Moreinis, I. Wagner and A. Kolodny, "Logic gates as Repeaters," Proceedings of IFIP conference on VLSI-SoC , Darmstadt, Germany, December 2003.

C11   N. Magen, A. Kolodny, U. Weiser and N. Shamir, "Interconnect-power dissipation in a Microprocessor," International System Level Interconnect Prediction workshop (SLIP 2004), Paris, February 2004.

C12   A. Morgenshtein, I. Cidon, A. Kolodny and R. Ginosar, "Comparative analysis of serial vs. parallel lings in NoC," Proceedings of 2004 International Symposium on System-on-Chip, pp. 185 – 188, Tampere, Finland, November 2004.

C13   M. Moreinis, A. Morgenshtein, I. A. Wagner and A. Kolodny, "Repeater Insertion combined with LGR Methodology for on-Chip Interconnect Timing Optimization," IEEE International Conference on Electronics, Circuits and Systems, Tel Aviv, December 2004.

C14   S. Michaely, S.l Wimer, and A. Kolodny, "Optimal Resizing of Bus Wires in Layout Migration," Proceedings of 11th IEEE International Conference on Electronics, Circuits and Systems, Tel Aviv, December 2004.

C15   A. Barger, D. Goren and A. Kolodny, "Design and Modeling of Network on Chip Interconnects," IEEE International Conference on Electronics, Circuits and Systems, Tel Aviv, December 2004.

C16   E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny, "Automatic and Hardware-Efficient SoC Integration by QoS Network on Chip," IEEE International Conference on Electronics, Circuits and Systems, Tel Aviv, December 2004.

C17   A. Morgenshtein, I. Cidon, A. Kolodny and R. Ginosar, "Micro-modem concept for communications in networks on chip," IEEE International Conference on Electronics, Circuits and Systems, Tel Aviv, December 2004.

C18   F. Chu, A. Kolodny, S. Maital and D. Perlmutter, "The innovation paradox: Reconciling creativity & discipline - How winning organizations combine inspiration with perspiration," Proceedings of IEEE International Engineering Management Conference, vol. 3 pp. 949-953, Singapore, October 2004.

C19   A. Morgenshtein, I.Cidon, A. Kolodny and R. Ginosar, "Low-Leakage Repeaters for NoC Interconnects," Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 600 - 603, May 2005.

C20   M. Popovich, E. G. Friedman, M. Sotman, and A. Kolodny, "On-Chip Power Distribution Grids with Multiple Supply Voltages for High Performance Integrated Circuits," Proceedings of the ACM Great Lakes Symposium on VLSI, pp. 2 – 7, April 2005 . (GLSVLSI Best Student Paper Award).

C21   S. T. Morad, U. Weiser and A. Kolodny, "Why Not Data Trace Cache," Workshop on Duplicating, Deconstructing, and Debunking (WDDD, Held in conjunction with ISCA-32), 2005.

C22   M. Behar, A. Mendelson and A. Kolodny, "Trace Cache Sampling Filter," 14th International Conference on Parallel Architectures and Compilation Techniques (PACT), pp. 255 – 266, 17-21 Sept. 2005.

C23   M. Sotman, M.Popovich, A. Kolodny and E.G. Friedman, "Leveraging Symbiotic On-Die Decoupling Capacitance," IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging (EPEP), pp. 111 – 114, October 2005.

C24   Z. Guz, I. Walter, E. Bololtin , I. Cidon, R. Ginosar and A. Kolodny, "Efficient Link Capacity and QoS Design for Wormhole Network-on-Chip," Proceedings of Design Automation and Test in Europe (DATE 2006), March 2006.

C25   R. Dobkin, R. Ginosar and A. Kolodny, "Fast Asynchronous Shift Register for Bit-Serial Communication," 12th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2006), 10 pp., March 2006.

C26 M. Sotman, A. Kolodny, M. Popovich and E. Friedman, "On-die Decoupling Capacitance: Frequency Domain Analysis of Activity Radius," Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 489 – 492, May 2006.

C27 M. Popovich, E.G. Friedman, M. Sotman, A. Kolodny and R.M. Secareanu, "Maximum effective distance of on chip Decoupling Capacitors in Power Distribution Grids," Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI, pp. 173 – 179, April/May 2006.

C28 K. Moiseev, S. Wimer and A. Kolodny, "Timing Optimization of Interconnect by Simultaneous Net-Ordering, Wire Sizing and Spacing," Proceedings of the IEEE International Symposium on Circuits and Systems, pp. 329-332, May 2006.

C29 A. Barger, D. Goren and A. Kolodny, "Simple Criterion for Maximizing Data Rate in NoC Links", 10th IEEE Workshop on Signal Propagation on Interconnects, Berlin, May 2006.

C30 A. Morgenshtein, A. Kolodny, R. Ginosar, "Link Division Multiplexing (LDM) for Network-on-Chip Links", IEEE 24th Convention of Electrical and Electronics Engineers in Israel, Israel, pp. 245-249, November 2006.

C31 A. Morgenshtein, A. Kolodny, R. Ginosar, "Asynchronous Bit-stream Compression, " IEEE 24th Convention of Electrical and Electronics Engineers in Israel, Israel, pp. 241-244, November 2006.

C32 K. Moiseev, S. Wimer and A. Kolodny, "An effective technique for simultaneous interconnect channel delay and noise reduction in nanometer VLSI design", IEEE 24th Convention of Electrical and Electronics Engineers in Israel, Israel, November 2006.

C33 R. Dobkin, Y. Perelman, T. Liran, R. Ginosar and A. Kolodny, "High rate wave-pipelined asynchronous on-chip bit-serial data link", Thirteenth IEEE International Symposium on Asynchronous Circuits and Systems, Berkeley, CA, March 2007 (ASYNC 2007).

C34 E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny, "Routing Table Minimization for Irregular Mesh NoCs", DATE 2007, Nice, France, March 2007.

C35 E. Bolotin, Z. Guz, I. Cidon, R. Ginosar and A. Kolodny, "The Power of Priority: NoC based Distributed Cache Coherency", NOCS 2007, Princeton, NJ, May 2007.

C36 I. Walter, I. Cidon, R. Ginosar and A. Kolodny, "Access regulation to Hot-Modules in Wormhole Networks", NOCS 2007, Princeton, NJ, May 2007.

C37 A. Morgenshtein, E. G. Friedman, R. Ginosar, and A. Kolodny, "Timing Optimization in Logic with Interconnect," Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction, pp. 19 - 26, April 2008.

C38 R. Dobkin, A. Morgenshtein, A. Kolodny, R. Ginosar, "Parallel vs. Serial On-Chip Communication," SLIP 2008, Newcastle, UK, April 2008 .

C39 Y. Aizik and A. Kolodny, "Exploration of Energy-Delay Tradeoffs in Digital Circuit Design," IEEEI 2008.

C40 Z. Guz, I. Keidar, A. Kolodny, and U. Weiser, "Utilizing Shared Data in Chip Multiprocessors with the Nahalal Architecture," 20th ACM Symp. on Parallelism in Algorithms and Architectures (SPAA'08), special track on Hardware and Software Techniques to Improve the Programmability of Multicore Machines, June 2008. (SPAA Best Paper Award).

C41 K. Moiseev, A. Kolodny and S. Wimer, "Wire Spacing, Planar Graphs and the Minimization of Dynamic Power in VLSI Microprocessors," VLSI-SOC 2008.

C42 I. Vaisband, E. Friedman, R. Ginosar and A. Kolodny, "Power Efficient Tree-Based Crosslinks for Skew Reduction," Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI, pp. 285 - 290, May 2009.

C43 R. Beraha, I. Walter, I. Cidon and A. Kolodny, "The Design of a Latency Constrained, Power Optimized NoC for a 4G SoC", NOCS 2009, San Diego, CA, May 2009.

C44 R. Manevich, I. Walter, I. Cidon and A. Kolodny, "Best of Both Worlds: A Bus-Enhanced NoC (BENoC)", NOCS 2009, San Diego, CA, May 2009.

C45 E. Krimer, M. Erez, I. Keslassy, A. Kolodny and I. Walter, "Packet-Level Static Timing Analysis for NoCs", NOCS 2009, San Diego, CA, May 2009.

C46 I. Walter, I. Cidon, and A. Kolodny, D. Sigalov, "The Era of Many-Modules SoC: Revisiting the NoC Mapping Problem", Second International Workshop on Network on Chip Architectures (NoCArc), 2010.

C47   Y. B. Itzhak, I. Cidon, and A. Kolodny, "Performance and Power Aware CMP Thread Allocation Modeling", International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC 2010), January 2010.

C48 K. Moiseev, A. Kolodny and S. Wimer, "Interconnect Power and Delay Optimization by Dynamic Programming in Gridded Design Rules," ISPD 2010.

C49 I. Walter, I. Cidon, and A. Kolodny, D. Sigalov, " Leveraging Application-Level Requirements in The Design of a NoC for a 4G SoC - a Case Study", DATE 2010.

C50 S. Beer, R. Ginosar, R. and A. Kolodny, "The Devolution of Synchronizers", ASYNC 2010, Grenoble, France, May 2010, pp. 94-103.

C51 A. Abdel-hadi, E.G. Friedman, R. Ginosar and A. Kolodny, " Timing–Driven Variation–Aware Nonuniform Clock Mesh Synthesis," Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI, pp. 15 - 20, May 2010.

C52 Z. Guz, O. Itzhak, I. Kediar. A. Kolodny, A. Mendelson and U.C. Weiser, "Threads vs. Caches: Modeling the Behavior of Parallel Workloads", ICCD 2010.

C53 T. Morad, A.Kolodny and U.C. Weiser, "Scheduling Multiple Multithreaded Applications on Asymmetric and Symmetric Chip Multiprocessors", PAAP 2010.

C54 R. Manevich, I. Cidon, A. Kolodny and I.Walter, "best of both worlds: A Bus Enhanced NoC", IEEEI 2010.

C55 S. Kvatinsky, E. G. Friedman , A. Kolodny and L. Schächter, "Power Grid Analysis Based on a Macro Circuit Model", IEEEI 2010.

C56 G. Sizikov, E.G. Friedman, A. Kolodny and M. Zelikson, Frequency Dependent Efficiency Model of On-Chip DC-DC Buck Converters", IEEEI 2010.

C57 G. Sizikov, E.G. Friedman, A. Kolodny and M. Zelikson, "Efficiency Optimization of Integrated DC-DC Buck Converters," ICECS 2010.

C58 T.Y. Morad, A. Kolodny and U.C. Weiser, "Scheduling Multiple Multithreaded Applications on Asymmetric and Symmetric Chip Multiprocessors," PAAP 2010.

C59 Y. Ben-itzhak, I. Cidon and A. Kolodny, "Delay Analysis of Wormhole Based Heterogeneous NoC," NOCS 2011.

C60 S. Beer, R. Ginosar, M. Priel, R. Dobkin, A. Kolodny, "An on-chip metastability measurement circuit to characterize synchronization behavior in 65nm", ISCAS 2011.

C61   Y. Ben-Itzhak, E. Zahavi, I. Cidon and A. Kolodny, "NoCs simulation framework for OMNeT++", NOCS 2011.

C62   S. Kvatinsky, E.G. Friedman, A. Kolodny and U. C. Weiser, "Memristor-based IMPLY Logic Design Procedure," ICCD 2011.

C63   R. Manevich, I.Cidon,A. Kolodny, I. Walter and S. Wimer, "Centralized Adaptive Routing for NoCs," EUROMICRO Conference on Digital System Design - DSD 2011.

C64   Y. Ben-Itzhak, E. Zahavi, I. Cidon and A. Kolodny, "HNOCS: Modular Open-Source Simulator for Heterogeneous NoCs,"   International Conference on Embedded Computer Systems (SAMOS) 2012.

C65   R. Malits, E. Bolotin, A. Kolodny and A. Mendelson, "Exploring the Limits of GPGPU Scheduling," HiPEAC 2012.

C66   Y. Ben-itzhak, I. Cidon and A. Kolodny , "Optimizing Heterogeneous NoC Design," SLIP 2012.

C67   R. Manevich, I. Cidon, and A. Kolodny, "Handling Global Traffic in Future CMP NoCs", SLIP 2012.

C68   S. Kvatinsky, E.G. Friedman, A. Kolodny and U. C. Weiser , "MRL - Memristor Ratioed Logic", CNNA 2012.

C69   E. Zahavi, I. Keslassy and A. Kolodny, "Distributed Adaptive Routing for Big-Data Applications Running on Data Center Networks", ANCS 2012.

C70   Y. Ben-Itzhak , I. Cidon and A. Kolodny, "Delay Analysis of Wormhole Based Heterogeneous NoC", IEEEI 2012.

C71   S. Kvatinsky, E.G. Friedman, A. Kolodny and U. C. Weiser , "The Desired Memristor for Circuit Designers," Nature Conference on Frontiers in Electronic Materials, Germany, June 2012.

C72   Y. Ben Itzhak, I Cidon and A. Kolodny," Delay Analysis of Wormhole Based Heterogeneous NoC," IEEEI 2012.

C73   R. Manevich, I. Cidon and A. Kolodny, "Handling Global Traffic in Future CMP NoCs," IEEEI 2012.

C74   S. Kvatinsky, K. Talisveyberg, D. Fliter, E. G. Friedman, A. Kolodny and U.C. Weiser, "Models of Memristors for SPICE Simulations," IEEEI 2012.

C75   I. Vaisband, E. G. Friedman, R. Ginosar, A. Kolodny, "Energy metrics for power efficient crosslink and mesh topologies", ISCAS 2012.

C76   S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "MRL - Memristor Ratioed Logic," Proceedings of the International Cellular Nanoscale Networks and their Applications, pp. 1-6, August 2012.

C77   R. Manevich, I. Cidon and A. Kolodny, "Dynamic Traffic Distribution Among Hierarchy Levels in Hierarchical Networks-on-Chip", NOCS 2013.

C78   R. Manevich, L. Polishuk, I. Cidon and A. Kolodny, "Design Tradeoffs of Long Links in Hierarchical Tiled Networks-on-Chip", EUROMICRO Conference on Digital System Design - DSD 2013.

C79   R. Manevich, S. Rehana, O. Turgeman and A. Kolodny, "ViLoCoN - An Ultra Lightweight Lossless VLSI Video Codec for NoC", SOCC 2013.

C80   S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memory Intensive Computing," Proceeding of the Annual Non-Volatile Memories Workshop, March 2014.

C81   O. Itzhak, I. Keidar, A. Kolodny and U. Weiser, "Performance scalability and dynamic behavior of Parsec benchmarks on many-core processors," SFMA 2014.

C82   S. Kvatinsky, Y. H. Nacson, R. Patel, Y. Etsion, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristive Multistate Pipeline Register," Proceedings of the International Cellular Nanoscale Networks and their Applications, July 2014.

C83   E. Zahavi, I. Keslassy, and A. Kolodny, "Quasi Fat Trees for Utility Clusters and their Fault-Resilient Closed-Form Routing," Hot Interconnects, 2014.

C84   E. Zahavi, O. Rottenstreich, A. Shpiner, I. Keslassy and A. Kolodny, "Links as a Service (LaaS): Feeling Alone on the Shared Cloud", ANCS 2016.

Invited Talks

T1   "Trends in CAD for VLSI," VLSI workshop, Eilat, Israel, 1990.

T2   "Life in the Synchronous Lane," Keynote presentation in ASYNC 2000 - International Symposium on Advanced Research in Asynchronous Circuits and Systems, Israel, April 2000.

T3   "Network on Chip", Keynote presentation in System Level Interconnect Prediction workshop (SLIP 2007), Austin, Texas, March 2007.

T4   "Threads, Caches and NoCs," ETNA - 1st International Workshop on Emerging Topics in NoC-aware Computer Architecture, ISCA 2013.

T5   "Power efficiency by system management and architecture", Intel's Annual Symposium on CAD and Validation, 2013.

T6   "The VLSI Interconnect Challenge", Symposium on Green Photonics, Technion 2014.

T7   "Power efficient System Architectures", Symposium on Green Photonics, TU Berlin 2015.

Invited papers and book chapters

I1   A. Kolodny, "Interconnects in ULSI systems", in Advanced Nano-Scale ULSI Interconnects - Fundamentals and Practice, Edited by Y. Shacham-Diamand et al., Springer 2009.

I2   R. Beraha, I. Walter, I. Cidon, and A. Kolodny, "Latency constrained Power Optimized NoC Design for a 4G SOC: A Case Study," in Low-Power NoCs, Edited by C. Silvano et al., Springer 2010.

I3   P. Gelsinger, D. Kirkpatrick, A. Kolodny and G. Singer, "Such a CAD! - Coping with complexity of microprocessor design at Intel," invited paper in IEEE Solid-State Circuits Magazine, vol.2, no.3, pp.32-43, 2010.

I4   S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "The Desired Memristor for Circuit Designers," IEEE Circuits and Systems Magazine, second quarter, pp. 17-22, May 2013.

I5   A. Kolodny, "Energy Eficcient System Architectures", in Green Photonics and Electronics, Edited by G. Eisenstein and D. Bimberg, Springer 2017.

Books

B1   K. Moiseev, A. Kolodny and S. Wimer, "Multi-Net Interconnect Optimization", ISBN 978-1-4614-0820-8, Springer 2015.

Technical reports (not published elsewhere)

1.   I. Kidron, S. Margalit, A. Kolodny and Y. Shacham, "Analysis of an Infrared Photoconductor with Focal-plane Integration," Technion Microelectronics Research Center, 1980.
2.   Tomer Y. Morad, Uri C. Weiser and Avinoam Kolodny, "ACCMP - Asymmetric Chip Multi-Processing ", CCIT Technical Report #488, June 2004.
3.   I. Sorani, A.Kolodny and A. Mendelson, "Usage of Trace Cache for Predicting Power Saving Opportunities, " Technion EE Pub No. 1665, CCIT Report #708, November 2008.

Textbook

1.   A. Kolodny, Computer-Aided Circuit Analysis with LISA (in Hebrew) Michlol, 1975.

Patents

1.   U.S. Patent 4,577,295, "Hybrid E2 Cell and Related Array," March 1986, by B. Eitan, A. Kolodny, D. Amrany and J. McCreary.
2.   U.S. Patent 4,785,199, "Programmable complementary transistors", November 1988, by A. Kolodny and Y. Brandman.
3.   Y. Elboim, A. Kolodny & R. Ginosar, "Clock tuning circuit in Chip Design," U.S. Patent application, December 2000.
4.   R. Dobkin, R. Ginosar, A. Kolodny and M. Moyal, "Current mode communication scheme," patent application, 2007.
5.   A. Morgenshtein, E. G. Friedman, R. Ginosar and A. Kolodny, "Unified Logical Effort - A Method for Delay Evaluation and Minimization in Logic Paths with RC Interconnect," patent application, 2008.
6.   I. Walter, I. Cidon and A. Kolodny, "Bus Enhanced Netowrk on Chip," patent application, 2008.
7.   A. Morgenshtein, R. Ginosar, A. Kolodny, and E. G. Friedman, " Logic Circuit Delay Optimization," United States Patent, No. 8,225,265, July 17, 2012.
8.   D. DiCastro, D. Soudry, S. Kvatinsky ,A. Gal, A. Kolodny "Analog multiplier using a memristive device and method for implemening Hebbian learning rules using memrisor arrays ", US Patent 9,659,650 B2 , 2017.
9.   A. Kolodny, S. Kvatinsky, R. Patel, E. Friedman, "Multistate register having a flip flop and multiple memristive devices", US Patent 9,754,203 B2, 2017.

10.   **Participation in Organizing Conferences**

2004 -   Technical Program Committee member, IEEE International Conference on Electronics, Circuits and Systems (ICECS 2004).

2005 -   Special session co-organizer (Repeater Insertion, IEEE ISCAS 2005).

2005 -   Review Commitee member for IEEE ISCAS 2006.

2005 -   Co-organizer of workshop on future interconnect and NoC (in DATE 2006).

2006 -   Program committee founding co-chairman, IEEE 1st International Symposium on Networks on Chips, Princeton University, May 2007.

2007 -   Member of the Steering Committee, IEEE International Symposium on Networks on Chips.

2008 -   SLIP program committee member, special sessions chair.

2008 -   VLSI-SoC 2008 conference program committee member.

2009 -   DATE 2009 - Network-on-Chip topic program committee member.

2009 -   NoC symposium TPC and steering committee member.

2010 -   NoC symposium TPC and steering committee member.

2010 -   IEEE Israel conference – special session organizer.

2011 -   NoC symposium TPC and steering committee member.

2012 -   IEEE Israel workshop on Memristors, Memristive Memory and Applications 2012, 2013, 2014, 2015 - NoC symposium TPC member.

2017 -   "Beyond CMOS – from Devices to Systems" – Seiden workshop, Technion