An effective technique for simultaneous interconnect channel delay and noise reduction in nanometer VLSI design

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***Abstract* – Capacitive coupling is the primary source of noise in nanometer technology digital CMOS VLSI circuits. It becomes worse with technology scaling. The interconnect capacitive crosstalk noise can be characterized by two parameters: peak noise voltage, and delay uncertainty. Delay uncertainty optimization can be seen as a subset of interconnect delay optimization. This paper addresses the problem of ordering and sizing parallel wires in a single metal layer within an interconnect channel of a given width, such that cross-capacitances are optimally shared for simultaneous noise and delay minimization. Using an Elmore delay model including cross capacitances for a bundle of wires and well-known crosstalk models, we show that "symmetric hill" wire ordering according to the strength of signal drivers, which is known to optimize channel timing characteristics, can be used also for minimizing channel noise metrics. Examples using state-of-the-art circuits in 65-nanometer technology are analyzed and discussed.**

1. INTRODUCTION

It is widely known that in recent generations of VLSI interconnect design has become a major concern as a result of technology scaling [12, 2]. As a result, cross-capacitance between wires in nanometer interconnect structures has turned out to be the dominant component of total net capacitance. High interconnect coupling leads to increase in circuit delay and crosstalk noise. Therefore, reducing of interconnect coupling capacitance is an important task in the view of both circuit noise and timing optimization.

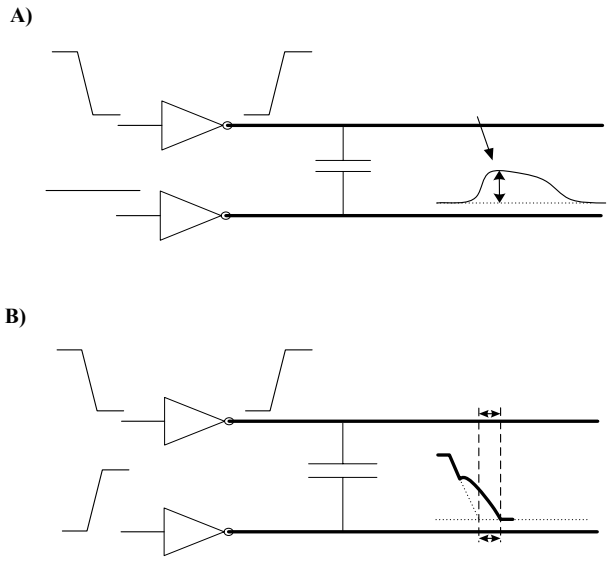

Figure 1 Crosstalk noise effects in VLSI circuits. A) peak noise; B) delay uncertainty

When talking about crosstalk noise, the net on which noise is being induced is called the *victim* net whereas the net that induces this noise is called the *aggressor* net. The noise between neighbor wires can cause two main problems in VLSI circuits. First of all, crosstalk noise can lead to logic malfunctions. This happens when voltage change on aggressor net causes voltage change on a "quiet" victim net, which might lead to eventual logic failure (Fig 1a). Such noise is quantified by *peak noise voltage* [3]. If noise is injected on the victim net during logic transition, it can modify the victim's waveform, causing *delay uncertainty* (Fig 1b) [4, 5, 6]. As a result, net delay becomes unpredictable and a non-critical path can become critical. Thus, uncertainty in path delays can cause significant degradation in clock frequency. Therefore, minimization of net delay uncertainty can be seen as a sub-task of circuit delay optimization.

Various methods have been proposed for crosstalk elimination and minimization. One of the most well-known methods is shield insertion [7], in which victim and aggressor are screened from each other by shield wires tied to either ground or power supply. Other methods are active shielding [8], repeater insertion [9, 10], device sizing [11, 12, 19], wire spacing [13, 14, 19] and different routing techniques [15-19].

Our technique for crosstalk noise optimization is based on simultaneous ordering and spacing of wires within an interconnect channel – a bundle of interconnect wires running in parallel between two "walls" (wires tied to ground or V_{dd}). The total width of the interconnect structure is a given constant and all wires in the channel are of the same length (Fig 2a). Such a model is very convenient for theoretical analysis but relatively rare in real industrial designs. The more common structure in practice is a non-uniform channel shown in Fig 2b. The optimization flow should be then as follows:

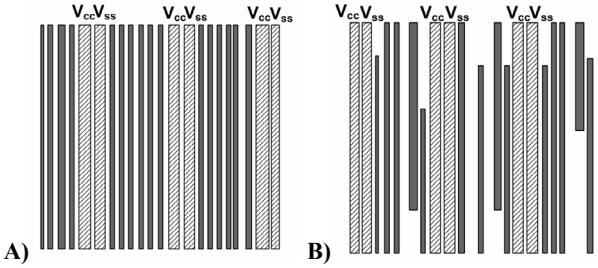

Figure 2 Interconnect channels (the walls of channels are dashed). A) homogenous channels; B) non-uniform channels

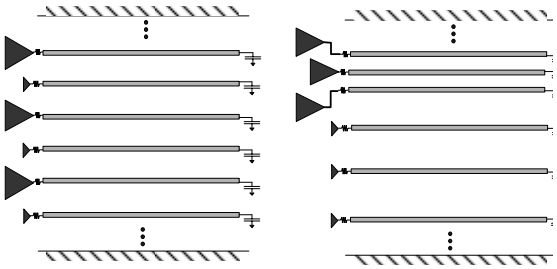

Figure 3 Two ways to order wires in an interconnect channel. "S" – strong drivers (small resistance), "W" – weak drivers (large resistance). Case A: interleaved placement, all wires share equal spaces. Case B: sorted placement, wires with weak drivers share large spaces and wires with strong drivers share small spaces, with improved circuit timing.

1) Transform non-uniform channels into homogenous ones;

2) Optimize the homogenous channels;

3) Convert the transformed channels back to non-uniform channels.

This paper focuses on the second stage of this flow.

Earlier, the authors showed that simultaneous wire ordering accordingly to wire driver can optimize delay characteristics of an homogenous channel [20]. The problem was motivated by the following example: two different arrangements of the same wires, presented in Fig.3 a and Fig.3 b result in different circuit timing, since in the second case inter-wire spaces are shared more effectively due to grouping of wires of each driver type together. The general ordering idea is to place drivers with similar strengths near each other in order to make them share high or low cross-capacitance. In crosstalk effects, the aggressor and driver are mostly defined by the strength of drivers of neighbor wires [19, 21, 22]. Wire with significantly stronger driver can cause large voltage spike on the neighbor wire. In order to minimize reciprocal effect of neighbor wires on each other, wire drivers are likely to be equalized. That is to say, in order to minimize crosstalk, wires with similar drivers should be placed near each other. This is analogous to ordering of wires for minimizing delay. Therefore, we assumed that the order of wires minimizing channel delay can also minimize channel noise characteristics.

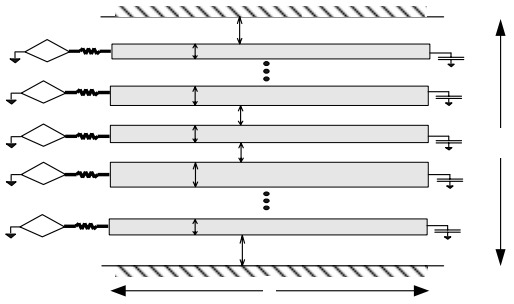

Figure 4 Interconnect configuration. The total channel width is A and the length is L. Each wire σ_i is of width W_i, with spaces to neighbors S_i and S_{i+1}, driven by a gate with effective resistance R_i and loaded by a gate with capacitance C_i.

Several other variants of net-reordering have already been applied for noise reduction, but not for delay reduction [3, 15, 18, 23, 24]. Vittal et al. [3] have suggested to reduce capacitive coupling noise by sorting wires in order of driver strength, which is closely related to our results. The strength of our technique is that it is based on more general approach – optimal sharing of inter-wire space – and thus effectively and simultaneously reduces both channel delay and noise characteristics.

The rest of this paper is organized as follows. In the section 2 formal problem definition is given. In section 3 the optimal order minimizing channel delay is presented and in section 4 its application to minimizing channel noise is shown. Section 5 brings simulation results and section 6 summarizes and concludes the paper.

2. PROBLEM FORMULATION

Circuit structure and notation are shown in Figure 4, illustrating n signal nets $\sigma_0,...,\sigma_{n-1}$ between two shield wires. S_i and S_{i+1}, respectively, denote spaces to the left and right neighbors of wire σ_i. W_i is the wire width. The length of all the wires is L. The total sum of wire widths and spaces is constrained to be A, representing the area available for laying out all of the signal wires.

$$g(\overline{W},\overline{S}) = \sum_{j=0}^{n-1} W_j + \sum_{j=0}^{n} S_j = A \qquad (2.1)$$

This is a common structure, which is amenable to simple mathematical analysis. Wires with repeaters can be segmented into several problem instances of this form. The delay Δ_i of signal σ_i can be calculated from the π-model equivalent circuit shown in Figure 5, where R_i is the effective output resistance of the driver, R_{W_i} is the wire resistance, C_{W_i} is the area and fringe capacitance, C_{C_i} and $C_{C_{i+1}}$ are the coupling capacitances to the left and right neighboring signals, and C_i is the capacitive load of the receiver's input.

Using an Elmore model with first order approximation for capacitances [**Error! Reference source not found.**25], the delay can be expressed as [**Error! Reference source not found.**26]:

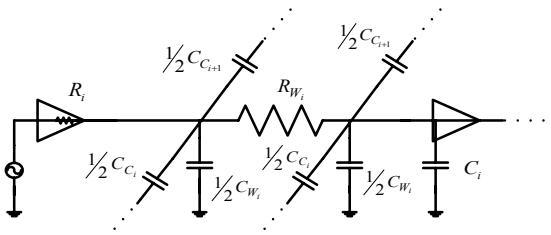

Figure 5 Equivalent circuit for calculating the i[th] signal delay

$$\Delta_i = (a + \frac{b}{W_i} + \frac{d}{W_i S_i} + \frac{d}{W_i S_{i+1}} + \frac{eC_i}{W_i} + kR_i W_i + gR_i + \frac{hR_i}{S_i} + \frac{hR_i}{S_{i+1}} + R_i C_i) \qquad (2.2)$$

where coefficients of wire widths, spaces, driver resistances and load capacitances are technology-dependent constants. Here we use expression for nominal wire delay, since we model wire delay uncertainty independently. Despite its simplicity, this Elmore-based modeling approach is widely used in practical interconnect optimizations. With empirical parameter tuning, the model accuracy can be improved further. In [**Error! Reference source not found.**], good absolute accuracy versus circuit simulation has been obtained. Interesting tradeoffs can be made because wire resistance and capacitance change in opposite directions as wire width grows, and increased spacing reduces

the side-capacitance shared by adjacent wires. Hence, wire reordering can change adjacency relations and affect the optimal allocation of spaces and wire widths.

Let f_1 given in (2.3) be the objective function we wish to minimize. f_1 denotes the sum of all signal delays. It is commonly used in early design stages since it captures the contributions of all signals to circuit timing.

$$f_1 = \sum_{i=0}^{n-1}\left(a + \frac{b}{W_i} + \frac{d}{W_i S_i} + \frac{d}{W_i S_{i+1}} + \frac{eC_i}{W_i} + \right. \\ \left. + kR_i W_i + gR_i + \frac{hR_i}{S_i} + \frac{hR_i}{S_{i+1}} + R_i C_i \right) \tag{2.3}$$

For final performance tuning, it is appropriate to speed-up the slowest signal. The objective function for such MinMax optimization is

$$f_2 = \max_{0\le i\le n-1}\left\{ a + \frac{b}{W_i} + \frac{d}{W_i S_i} + \frac{d}{W_i S_{i+1}} + \frac{eC_i}{W_i} + kR_i W_i + \right. \\ \left. + gR_i + \frac{hR_i}{S_i} + \frac{hR_i}{S_{i+1}} + R_i C_i \right\} \tag{2.4}$$

When required times of signals are specified, the corresponding objective functions are sum of slacks and the worst slack among all signals. Minimizing the sum of slacks is equivalent to minimizing f_1. The case of minimizing worst slack can be transformed to minimizing worst wire delay f_2.

For calculating crosstalk noise effectively, several models have been presented in the literature [3, 6, 27, 28]. For peak noise V_p we use relatively simple model, given in [3]. According to it, the peak noise on wire i can be represented as

$$V_p = V_{dd}\,\frac{R_i \cdot C_{c_i} + R_{w_i} \cdot \dfrac{C_{c_i}}{2}}{\Delta_{i-1} + \Delta_i + \Delta_{i+1}} \tag{2.5}$$

In (2.5), the numerator represents a part of wire delay caused by coupling capacitance and the denominator represents the sum of Elmore delays of the wire and its neighbors. Rewriting (2.5) in terms of (2.2), obtain

$$V_{p,i} = V_{dd}\,\frac{\left(\dfrac{d}{W_i} + hR_i\right)\cdot\left(\dfrac{1}{S_i} + \dfrac{1}{S_{i+1}}\right)}{\Delta_{i-1} + \Delta_i + \Delta_{i+1}},\quad 0 < i < n-1$$

$$V_{p,0(n-1)} = V_{dd}\,\frac{\left(\dfrac{d}{W_{0(n-1)}} + hR_{0(n-1)}\right)\cdot\left(\dfrac{1}{S_{0(n-1)}} + \dfrac{1}{S_{1(n)}}\right)}{\Delta_{0(n-1)} + \Delta_{1(n)}} \tag{2.6}$$

For analytically modeling the delay uncertainty caused by effects of crosstalk noise on circuit timing, we use superposition-based approximations, proposed in [29]. According to it, the upper bound of peak noise of wire i can be expressed as

$$\delta_{\max,i} = \Delta_i \ln\left(2\frac{V_{p,i}}{V_{dd}} + 1\right) \tag{2.7}$$

Now introduce two new objective functions:

$$f_3 = \sum_{i=0}^{n-1} \delta_{\max,i} \tag{2.8}$$

and

$$f_4 = \max_i \delta_{\max,i} \tag{2.9}$$

The meaning of these objectives is similar to the meaning of objectives (2.3) and (2.4). In the first case, we are interested in crosstalk minimization over all wires in a channel, while in the second case criticality of some nets is known.

3. DELAY OPTIMIZATION

In this section, we present optimal order minimizing delay objectives f_1 and f_2 (2.3-2.4). In the next section, we show that the same order can optimize also noise objectives f_3 and f_4 (2.8-2.9)

Let each wire have width W_i assigned as follows:

$$W_i = \frac{1}{\psi(R_i)}, \tag{3.1}$$

where ψ **is a monotonically non-decreasing** functions of driver resistance R_i. Such assignment is practically common, as one attempts to balance the resistance of the driver and the resistance of the driven line and is equivalent to impedance matching. Notice that the case of uniform width wires is also covered by (3.1). The solution of minimizing f_1 under the constraint g (in (2.1)) implies optimal order, called Symmetric Hill Order, which depends only on driver resistances, while the effect of load capacitances is order-insensitive [20].

We now describe how to obtain the optimal order. The driver with the largest resistance is taken to reside at the center of the channel. The other drivers are taken in monotonically decreasing order of driver resistance, and located alternately on the left and right of as shown in Figure 6. The advantage of such order stems from the fact that spaces are shared by wires with similar driver resistances, since the side-capacitance to the sidewalls can be modeled as capacitance to ground, hence the sidewalls affect our model as if they were wires with zero-resistance drivers.

In the most general case, both wire widths and spaces can vary arbitrarily, yielding $2n+1$ equations. In this case the optimal wire ordering may depend on the values of capacitive loads and is not necessarily Symmetric Hill. The next theorem defines conditions for optimality of Symmetric Hill order in the most general case.

Theorem: For a given set of n wires, if each pair of wires σ_i and σ_j with driver resistances and load capacitances (R_i, C_i) and (R_j, C_j) satisfy $R_i > R_j$ and $C_i \le C_j$, then the optimal order of this set of wires is Symmetric Hill, under total sum of wire delays objective function.

If the conditions of the theorem are met there is no need to constrain wire width by function $\psi(R)$; in the other case the solution of the most general problem is very complex, as it involves the exploration of many permutations.

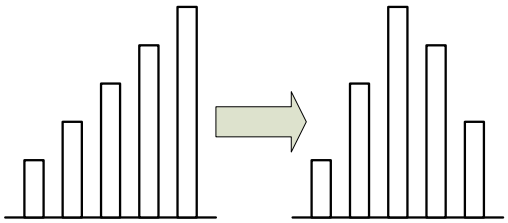

Figure 6 Building Symmetric Hill Order from a set of wires sorted according to driver resistance

In order to make the computational effort reasonable, the following heuristic is proposed. It is based on the Symmetric Hill Order and yields near-optimal solutions. The complex optimization problem is divided into two successive simpler ones. First, the above theorem is checked. If it is satisfied, the optimal order is Symmetric Hill and wire sizing and spacing are performed by continuous optimization [**Error! Reference source not found.**30]. Otherwise, the heuristic assigns wire widths by some parameterized monotonic non-increasing function (3.1). Symmetric Hill order is now guaranteed to be optimal. Then continuous optimization is applied [**Error! Reference source not found.**30], exploring for the optimal values of inter-wire spaces and the width-function parameters. This heuristic reduces time complexity of the optimization problem by factor of $O(n!)$ and reduces the number of unknown parameters from $2n+1$ to $n+p$, where p is the number of parameters in the width function. Experiments show that a well-chosen width-function yields ordering, widths and spaces that result in total sum of delays which is very close to the global optimum.

Since (2.4) is not differentiable, the technique used for deriving optimal order for total sum of delays cannot be applied for minimization of worst wire delay. We have demonstrated experimentally that Symmetric Hill order is optimal under maximum delay objective in most cases. We have created about 1000 random problem instances for 5 wires and 100 random problem instances for 6 wires and obtained Symmetric Hill optimal order in most cases (the computational effort is infeasible for a larger number of wires). These results are described in details in [20].

4. CROSSTALK NOISE OPTIMIZATION

Because of the high complexity of delay uncertainty expressions the technique used for obtaining optimal order in sum of delays minimization cannot be applied here. However, using stated below observations and following experiments we demonstrate that Symmetric Hill order is optimal for delay uncertainty minimization in most cases.

First, we simplify the expression for V_p. For many real cases it can be assumed that $V_p / V_{DD} << 1$ [21, 29, 31]. Therefore, the following Taylor approximation is applicable:

$$\ln\left(2\frac{V_p}{V_{dd}}+1\right)\approx\frac{2\cdot V_p}{V_{dd}}.$$

By substituting to (2.7), obtain:

$$\delta_{\max,i}=\frac{2\cdot\Delta_i\cdot V_{p,i}}{V_{dd}}=$$

$$=2\cdot\frac{\Delta_i}{\Delta_{i-1}+\Delta_i+\Delta_{i+1}}\left(\frac{d}{W_i}+hR_i\right)\cdot\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right) \quad (3.2)$$

The expressions for delay uncertainty of boundary wires are obtained similarly.

Accordingly to (3.5), objectives (2.8) and (2.9) become

$$f_3=2\sum_{i=1}^{n-1}\frac{\Delta_i}{\Delta_{i-1}+\Delta_i+\Delta_{i+1}}\left(\frac{d}{W_i}+hR_i\right)\cdot\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right) \quad (3.3)$$

and

$$f_4=2\max_i\frac{\Delta_i}{\Delta_{i-1}+\Delta_i+\Delta_{i+1}}\left(\frac{d}{W_i}+hR_i\right)\cdot\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right) \quad (3.4)$$

In last two expressions the boundary terms are again eliminated.

Let's denote

$$q_i=\frac{\Delta_i}{\Delta_{i-1}+\Delta_i+\Delta_{i+1}} \quad (3.5)$$

It is known that in worst wire delay minimization all wire delays are equal [30]. Therefore, the ratios (3.8) are constant and equal to 1/3 (1/2 for boundary wires) Hence, both (3.6) and (3.7) reduce to minimization of sum or maximum of terms $\left(\frac{d}{W_i}+hR_i\right)\cdot\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right)$. These terms represent the part of wire delay resulting from cross-coupling capacitance and under assumption of (3.1) both (3.6) and (3.7) can be effectively minimized by Symmetric Hill Order. On the other hand, in total sum of delay minimization the ratios (3.8) are not constant values. However, when the channel is sorted in Symmetric Hill Order, wires with similar delays are placed near each other and, therefore, values of ratios (3.8) will be monotonic with wire resistances. Thus, they can be represented by $q_i=kR_i$, where k is some constant. Using this fact, minimization of (3.6) and (3.7) can be again reduced to minimization of terms $\left(\frac{d}{W_i}+hR_i\right)\cdot\left(\frac{1}{S_i}+\frac{1}{S_{i+1}}\right)$.

Thus, arranging channel in Symmetric Hill Order effectively minimizes both channel delay (total sum of delays or worst wire delay) and channel noise (total sum of delay uncertainties or worst wire delay uncertainty) characteristics.

5. RESULTS AND DISCUSSION

Numerical experiments for various problem instances were performed using 65 nanometer technology parameters calculated based on data derived from real industrial circuits. As we have discovered from real industrial data, typical cases of interconnect channels include up to 10 wires due to intensive shielding, therefore in all experiments we used small number of wires (the computational effort is infeasible even for number of wires larger than 5). Since timing optimization results have already been reported in [20], here we focus on noise optimization results. We evaluated 20 random problem instances using five signals. Each signal was assigned a driver randomly. The range of driver resistances was 100 Ω to 2 $K\Omega$ and load capacitances in the range 200 fF to 10 fF were assigned accordingly. For each problem the wire widths and spaces were optimized to yield minimum total sum of delays and minimum worst wire delay. This was done for all the 5! =120 possible order permutations. The procedure was repeated for five different channel widths A 2, 5, 8, 12 and 20 μm, and five different lengths L – 300, 500, 800, 1200 and 1500 μm. For best and worst orders total sum of delay uncertainties and maximum delay uncertainty were calculated. The results for

total sum of delays optimization and worst wire delay optimization are presented in tables 1 and 2 respectively. In each cell, the upper half cell (colored in gray) represents improvement in total sum of delay uncertainties and the lower half cell – improvement in maximum delay uncertainty. The experiment demonstrates that net ordering can significantly improve channel noise immunity. The maximum delay uncertainty is affected more than sum of delay uncertainties.

Table 1
Percent of average improvement (best vs. worst ordering) for random problem instances, in sum-of-delays optimization (upper half-cell – total sum of delay uncertainties, lower half-cell – maximum delay uncertainty)

	A= 2µm	A=5 µm	A= 8µm	A= 12µm	A= 20µm
L=300 µm	21.9	27.1	28.8	31.3	38.6
	26.6	32.2	38.2	48.1	46.7
L = 500 µm	22.1	26.9	28.4	30.6	32.6
	29.1	30.5	39.3	45.2	39.8
L = 800 µm	22.8	28.6	28.7	32.5	33.8
	28.3	34.7	38.4	36.6	44.1
L = 1200 µm	23.5	27.7	29.2	34.4	33.4
	25.3	30.7	37.0	41.2	38.9
L =1500 µm	24.1	27.6	29.9	34.4	29.3
	24.8	30.5	37.2	37.1	39.9

Table 2
Percent for average improvement (best vs. worst ordering) for random problem instances, in worst delay optimization (upper half-cell – total sum of delay uncertainties, lower half-cell – maximum delay uncertainty)

	A= 2µm	A=5 µm	A= 8µm	A= 12µm	A= 20µm
L=300 µm	21.8	27.2	29.0	30.3	35.4
	28.6	30.6	33.8	44.9	47.9
L = 500 µm	22.8	28.0	29.1	30.2	34.5
	28.2	31.9	39.6	46.6	41.6
L = 800 µm	22.2	29.1	28.3	30.2	35.5
	27.6	29.1	38.7	41.0	35.3
L = 1200 µm	24.1	28.8	30.5	33.3	33.5
	27.9	27.1	36.9	43.1	38.7
L =1500 µm	23.2	28.4	30.3	32.1	30.4
	27.0	31.6	33.6	43.4	38.0

6. CONCLUSION

We have shown that wire reordering technique for a wiring channel of constrained width, which was successfully used in the past for timing optimization, can also improve results of crosstalk noise optimization. The optimal order of wires generally depends on both wire driver resistances and load capacitances. Optimization of delay uncertainty is directly related to optimization of wire delay and can be seen as a subset of interconnect delay optimization. Numerical experiments demonstrated that arranging wires inside a channel in Symmetric Hill Order can improve total sum of delay uncertainties by 29.1% and maximum delay uncertainty by 35.9%

REFERENCES

1. R. Ho, K. Mai, and M. Horowitz, “The future of wires”, Proceedings of the IEEE, Vol. 89, no. 4, Apr. 2001
2. D. Sylvester and K. Keutzer, “Getting to the bottom of deep submicron”, *Proc. ICCAD*'98, pp. 203-211, 1998
3. A.Vittal, L Chen, M. Marek-Sadowska, K. Wang, and S Yang, “Crosstalk in VLSI Interconnections”, *IEEE Transactions on CAD Design of IC and Systems*, Vol.18, No. 12, Dec. 1999
4. T. Sato, Y. Cao, K. Agarwal, D. Sylvester, and C. Hu, "Bidirectional Closed-Form Transformation Between On-Chip Coupling Noise Waveforms and Interconnect Delay Change Curves", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, pp. 560-572, March 2003
5. O. Milter, A. Kolodny, "Crosstalk noise reduction in synthesized digital logic circuits", *IEEE transactions on VLSI*, pp. 1153-1158, Dec. 2003
6. A. Kahng, S. Muddu, and D. Vidhani, "Noise and Delay Uncertainty Studies for Coupled RC Interconnects", *Proc. of Twelfth Annual IEEE International ASIC/SO SOC Conference*, pp. 3-8, Sept. 1999
7. T. Xue, E. S. Kuh, and D. Wang, “Post Global Routing Crosstalk Risk Estimation and Reduction,” *Proc. ICCAD'96*, pp. 302-309, 1996
8. H. Kaul, D. Sylvester, and D. Blaauw, "Clock Net Optimiation using Active Shielding", *ACM/IEEE International Symposium on Low-Power Electronics Design*, pp. 265-268, 2003
9. C. Alpert and A. Devgan, "Buffer Insertion for noise and delay optimization", *IEEE Trans. Computer-Aided Design*, vol. 18, pp. 1633-1645, 1999
10. D. Li, A. Pua, P. Srivastava, and U. Ko, "A repreater optimization methodology for deep sub-micron, high performance processors", *Proc. ICCD*'97, pp. 726-731, 1997
11. T. Xiao and M. Marek-Sadowska, "Gate sizing to eliminate crosstalk induced timing violation", *Proc. ICCD*, pp. 186-191, 2001
12. M, Becer, D. Blaauw, O.Chanhee, I.Hajj, Z. Jingyan, R. Levy, S. Sirichotiyakil, and V. Zolotov, "A global driver sizing tool for functional crosstalk noise avoidance", *Proc. ISQED'02*, pp. 158-163, 2002
13. H. Chen and C. Wong, "Wiring and Croostalk Avoidance in Multi-Chip Module Design", *Proc. CICC'92*, pp. 28.6.1-28.6.4, 1992
14. K. Chaudhary, A. Onozawa, and E. Kuh, "A spacing Algorithm for Performace Enhancement and Cross-Talk Reduction", *Proc. ICCAD'93*, pp. 697-702, 1993
15. D. Kirkpatrik and A. Sangiovanni-Vincentelli, "Techniques for crosstalk avoidance in the physical design of high-performance digital systems", *Proc. ICCAD'94*, pp. 616-620, 1994
16. T. Zhang and S. Sapatnekar, "Simultaneous Shield and Buffer Insertion for Crosstalk Noise Reduction in Global Routing", *Proc. ICCD'04*, pp. 93-98, 2004
17. L. Li, N. Vijaykrishnan, M. Kandemir, and M. Irwin, "A Crosstalk Aware Interconnect with Variable Cycle Transmission", *Proc. DATE'04*, February, 2004
18. T. Gao and C. Liu, “Minimum Crosstalk Channel Routing”, *Technical Digest Int. Conf. on CAD*, pp. 692-696, 1993
19. M. Becer, D. Blaauw, V.Zolotov, R. Panda, and I. Hajj, "Analysis of Noise Avoidance Techniques in DSM Interconnects Using a Complete Crosstalk Noise Model", *Proc. DATE'02*, pp. 456-463, March 2002
20. K. Moiseev, S. Wimer, and A. Kolodny, "Timing optimization of interconnect by simultaneous net-ordering, wire sizing and spacing", *Proc. ISCAS'06*, pp. 329-332, May 2006
21. A. Vitall and M. Marek-Sadowska, "Crosstalk reduction in VLSI*", IEEE Tans.CAD, pp. 560-572*, March 2003
22. O. Milter, A. Kolodny, " Crosstalk noise reduction in synthesized digital logic circuits", IEEE transactions on VLSI, pp. 1153 – 1158, Dec. 2003
23. P. Gupta and A. Kahng. "Wire Swizzling to Reduce Delay Uncertainty Due to Capacitive Coupling." *Proc. IEEE Intl. Conf. on VLSI Design*, January, p.431, 2004
24. J. Ma and L. He, "Formulae and Applications of Interconnect Estimation Considering Shield Insertion and Net Ordering", *2001 International Conference on Computer-Aided Design (ICCAD '01)*, pp. 327-332, Nov. 2001
25. S. Wong, G. Lee and D. Ma, "Modeling of Interconnect, Capacitance, Delay and Crosstalk in VLSI", *IEEE Transactions on Semiconductor Manufacturing*, vol. 13, no.1, pp. 108-111 Feb. 2000
26. A. Abou-Seido, B. Nowak and C. Chu, “ Fitted Elmore Delay: A Simple and Accurate Interconnect Delay Model*”, IEEE Transactions on VLSI Systems*, vol. 12, no. 7, pp. 691-696, July 2004
27. T. Sakurai, "Closed-form expressions for interconnect delay, coupling, and crosstalk in VLSI's", IEEE Trans. Electron Devices, vol. 40, pp. 118-124, Jan 1993
28. J. Cong, D. Pan, and P. Srinivas, "Improved crosstalk modeling for noise constrained interconnect optimization", *Proc. ACM/IEEE Int. Workshop Timing Issues*, Austin , Texas, 2000
29. T. Sato, Y. Cao, D. Sylvester, and C. Hu, "Characterization of interconnect coupling noise using in-situ delay change curve measurements", *Proc. IEEE ASIC/SoC Conf.*, pp. 321-325, 2000
30. S. Michaely, S. Wimer and A. Kolodny, " Optimal resizing of bus wires in layout migration", *Proc. ICECS 2004*, pp. 411-414, 2004
31. T. Tang, E. Friedman, "Peak noise prediction in loosely coupled interconnect", Proc. ISCAS'99, vol. 1, pp. 541-544, 1999