On-Chip Power Distribution Grids with Multiple Supply Voltages for High Performance Integrated Circuits

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ABSTRACT

Multiple supply voltages are often utilized to decrease power dissipation in high performance integrated circuits. On-chip power distribution grids with multiple supply voltages are discussed in this paper. A power distribution grid with multiple supply voltages and multiple grounds is presented. The proposed power delivery scheme reduces power supply voltage drops as compared to conventional power distribution systems with dual supplies and a single ground by 17% on average (20% maximum). For an example power grid with decoupling capacitors placed between the power supply and ground, the proposed grid with multiple supply and multiple ground exhibits, respectively, 13% and 18% average performance improvement. The proposed power distribution grid can be an alternative to a single supply voltage and single ground power distribution system.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: Miscellaneous—*power distribution grids, power distribution systems, multiple power supply voltages, decoupling capacitors*

General Terms

Design

Keywords

Power distribution systems, power distribution grids, multiple power supply voltages, decoupling capacitors

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1. INTRODUCTION

With a new era of nanometer scale circuits, power dissipation has become a critical design issue. To manage the problem of high power dissipation, the use of multiple on-chip power supply voltages has been proposed [1]. This strategy has the advantage of allowing modules along the critical paths to operate with the highest available voltage level (in order to satisfy target timing constraints) while permitting modules along the noncritical paths to use a lower voltage (thereby reducing energy consumption). In this manner, the energy consumption is decreased without affecting circuit speed. This scheme to enhance speed results in smaller area as compared to the use of parallel architectures. The problem of using multiple supply voltages for reducing power requirements has been investigated in the area of high level synthesis for low power [2,3]. While it is possible to provide many supply voltages, in practical applications such a scenario is expensive. Practically, a small number of voltage supplies (two or three) is available.

Power distribution networks in high performance ICs are commonly structured as a multilayer grid [4]. In such a grid, straight power/ground lines in each metalization layer can span an entire die and are orthogonal to the lines in adjacent layers. Power and ground lines typically alternate in each layer. Vias connect a power (ground) line to another power (ground) line at the overlap sites. A typical on-chip power grid is illustrated in Fig. 1, where three layers of interconnect are depicted with the power lines shown in dark grey and the ground lines shown in light grey.

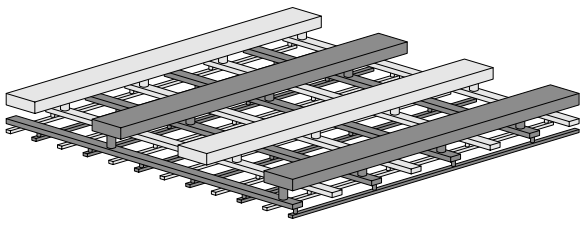


Figure 1: A multi-layer on-chip power distribution grid [5]. The ground lines are light grey, the power lines are dark grey. The signal lines are not shown.

Several design methodologies using multiple power supply voltages have been described in the literature. A row by row optimized power supply scheme, which provides a

different supply voltage to each cell row, is described in [6]. The original circuit is partitioned into two sub-circuits by conventional layout methods. Another technique presented in [7] decreases the total length of the on-chip power and ground lines by applying a multiple supply voltage scheme. A layout architecture exploiting multiple supply voltages in cell-based arrays is described in [8]. Three different layout architectures are analyzed. The authors show that power consumed by an IC can be reduced, albeit with an increase in area. In all previously reported works, only power distribution systems with two power supply voltages and one common ground have been described. An on-chip power distribution grid with multiple power supply voltages and multiple grounds is proposed in this paper.

The paper is organized as follows. The extracted structure of a power distribution grid and the simulation setup are described in Section 2. The structure of a power distribution grid with dual supply voltages and dual grounds (DSDG) is proposed in Section 3. Simulation results are presented in Section 4. Some specific conclusions are summarized in Section 5.

2. SIMULATION SETUP

The inductance extraction program FastHenry [9] is used to analyze the inductive properties of the on-chip power grids. FastHenry efficiently calculates the frequency dependent self and mutual impedances, $R(\omega)+\omega L(\omega)$, in complex three-dimensional interconnect structures. A magnetoquasistatic approximation is utilized, meaning the distributed capacitance of the line and any related displacement currents associated with the capacitances are ignored. The accelerated solution algorithm employed in the program provides approximately a 1% worst case accuracy as compared to directly solving the system of linear equations characterizing the system.

Copper is used as the interconnect material with a conductivity of $(1.72\,\mu\Omega{\cdot}\mathrm{cm})^{-1}$. A line thickness of 1 μm is assumed for all lines in the grids. In the analysis, the lines are split into multiple filaments to account for the skin affect. The number of filaments are estimated to be sufficiently large to achieve a 1% accuracy. Simulations are performed assuming a 1 GHz signal frequency. All of the interconnect structures are composed of interdigitated power and ground lines as shown in Fig. 2. The total number of lines in each power grid is 24. All of the lines dedicated to a particular power distribution network are distributed equally between the power and ground paths. The maximum simulation time is under 5 minutes on a Sun Blade 100 workstation.

3. POWER DISTRIBUTION GRID WITH DUAL SUPPLY AND DUAL GROUND

Multiple power supply voltages have been widely used in modern high performance ICs such as microprocessors to decrease power dissipation. Power delivery systems with dual power supply voltages are analyzed in this section. Only power distribution schemes with dual supply voltages and a single ground (DSSG) have been reported in the literature. In such networks, both power supplies share one common ground. The ground bounce produced by one power supply therefore adds to the power noise at the other power supply. As a result, voltage fluctuations at a particular current load is significantly increased. To address this problem, an on-chip power distribution scheme with DSDG is proposed. In this way, the power distribution system consists of two independent power delivery networks.

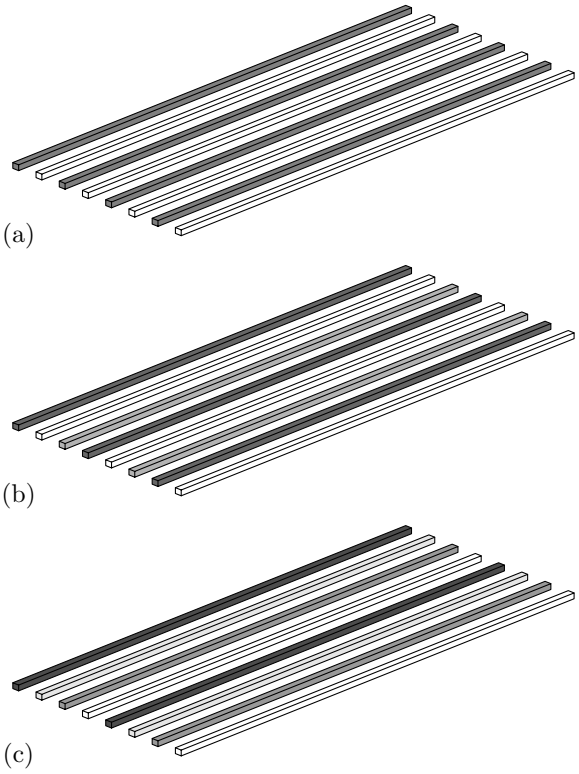


Figure 2: Power distribution grids under investigation. In all of the power distribution structures, the power lines are interdigitated with the ground lines. (a) A reference power distribution grid with a single supply voltage and a single ground (SSSG). The power lines are grey colored and the ground lines are white colored, (b) a power distribution grid with DSSG. The power lines are light and dark grey colored and the ground lines are white colored, (c) the proposed power distribution grid with DSDG. The power lines are shown in black and dark grey colors and the ground lines are shown in white and light grey colors.

A power distribution grid with DSDG consists of two separate subnetworks with independent power supply voltages and current loads. No electrical connection exists between the two power delivery subnetworks. In such a structure, the two power distribution systems are only coupled through the mutual inductance of the ground and power paths, as shown in Fig. 3.

The loop inductance of the current loop formed by the two parallel paths is

$$L_{loop} = L_{pp} + L_{gg} - 2M, \tag{1}$$

where L_{pp} and L_{gg} are partial self inductances of the power and ground paths, respectively, and M is the mutual inductance between these paths. The currents in the power and ground lines are assumed to always flow in opposite direc-

tions. The inductance of the current loop formed by the power and ground lines is therefore reduced by $2M$. The loop inductance of the power distribution grid can be further reduced by increasing the mutual inductive coupling between the power and ground lines. The mutual inductance between two parallel straight lines of equal length is [10]

$$M_{loop} = 0.2l\left(\ln\frac{2l}{d} - 1 + \frac{d}{l} - \ln\gamma + \ln k\right)\mu\text{H}, \qquad (2)$$

where l is the line length, and d is the distance between the line centers. This expression is valid for the case where $l \gg d$. The mutual inductance of two straight lines is a weak function of the distance between the lines [4].

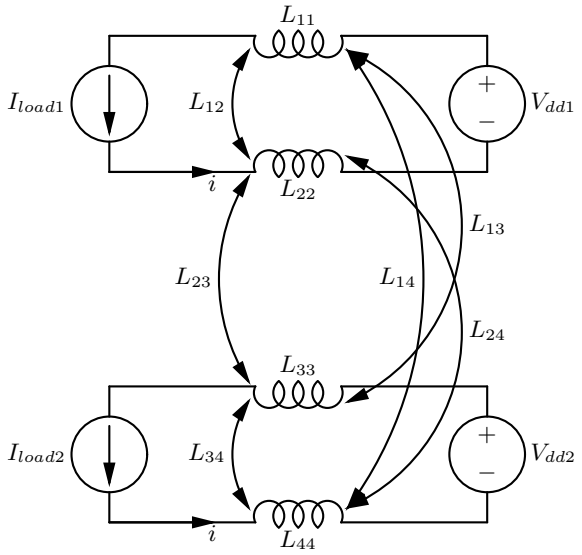


Figure 3: Circuit diagram of the mutual inductive coupling of the proposed power distribution grid. L_{11} and L_{33} denote the partial self inductances of the power lines and L_{22} and L_{44} denote the partial self inductances of the ground lines, respectively.

Analogous to inductive coupling between two parallel loop segments as described in [11], the mutual loop inductance of the two power distribution grids with DSDG is

$$M_{loop} = |L_{13} - L_{14} + L_{24} - L_{23}|. \qquad (3)$$

Note that different signs before the mutual inductances in (3) correspond to currents in the power and ground paths flowing in opposite directions. If the distance between the lines making a loop is much smaller than the separation between the two loops, $L_{13} \approx L_{14}$ and $L_{23} \approx L_{24}$. This situation is the case for paired power distribution grids. In such grids, the power and ground lines are located in pairs in close proximity. For the interdigitated grid structure shown in Fig. 2(c), the distance between lines d_{12} is the same as an offset between two loops d_{23}, as illustrated in Fig. 4. In this case, assuming $d_{12} = d_{23} = d$, from (2), M_{loop} between the two grids is approximately

$$M_{loop} = \left|0.2l\ln\frac{3}{4}\right| \ \mu\text{H}. \qquad (4)$$

Thus, the M_{loop} between the two grids is greater than zero in grids with DSDG. The loop inductance of the particular power distribution grid, therefore, can be further lowered by $2M$. Conversely, in grids with DSSG, currents in both power paths flow in the same direction. In this case, the resulting partial inductance of the current path formed by the two power paths is

$$L_{||} = \frac{L_{pp}^1 L_{pp}^2 - M^2}{L_{pp}^1 + L_{pp}^2 - 2M}, \qquad (5)$$

where L_{pp}^1 and L_{pp}^2 are partial self inductances of the two power paths, respectively, and M is the mutual inductance between these paths. The mutual inductance between two loops is increased. Thus, the loop inductance seen from a particular current load increases, producing larger power/ground voltage fluctuations.

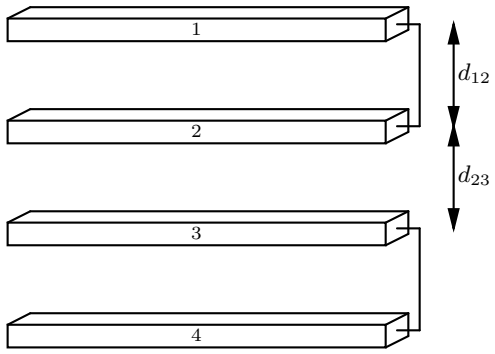


Figure 4: Physical structure of a power distribution grid with DSDG. The current loops represent two independent power delivery networks.

4. SIMULATION RESULTS

To model voltage fluctuations as seen from the current load, the power distribution grids are represented by ten series RL segments. It is assumed that both power delivery subnetworks are similar and source similar current loads. Two equal current loads are applied to the power grid with a single supply voltage and single ground (SSSG). A triangular current source with 50 mA amplitude, 100 ps rise time, and 150 ps fall time is applied to each grid in the power distribution network. No skew between the two current loads is assumed, modeling the worst case scenario with the maximum power noise. For each grid structure, the width of the lines varies from 1 μm to 10 μm, maintaining the line separation S_0 at a constant value of 1 μm. The maximum voltage sag from V_{dd} is estimated from SPICE for different line widths.

The performance of the proposed power distribution grid is quantitatively compared to the power noise of a conventional power distribution scheme with DSSG in subsection 4.1. The maximum voltage drop from V_{dd} for power distribution grids with decoupling capacitors is evaluated in subsection 4.2. Both power distribution schemes are compared to the reference power distribution grid with SSSG. The dependence of power noise on the switching frequency of the current loads is discussed in subsection 4.3.

4.1 Power Distribution Grids without Decoupling Capacitors

The maximum voltage drop for the three different power distribution grids without decoupling capacitors is depicted in Fig. 5. For all of the power distribution grids, the maximum voltage drop decreases sublinearly as the width of the lines is increased. This noise voltage drop is caused by the decreased loop impedance. The resistance of the metal lines decreases linearly with an increase in the line width. The loop inductance increases slowly as the line width increases. As a result, the total impedance of each of the power distribution schemes decreases sublinearly, approaching a constant impedance as the lines become very wide.

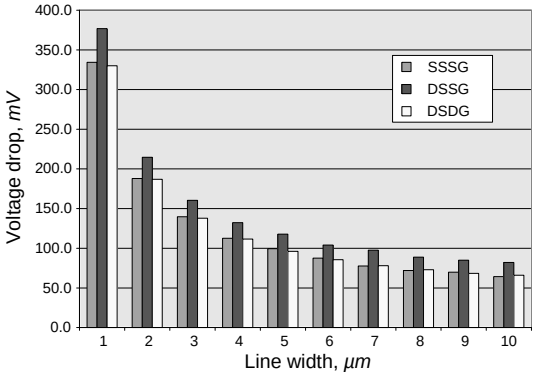


Figure 5: Maximum voltage drop for three types of power distribution grids. No decoupling capacitors are added.

As described in Section 3, the power distribution scheme with DSDG produces on average a 16.8% lower voltage drop as compared to the scheme with DSSG. The maximum improvement in noise reduction is 20% which is achieved for a 7 μm wide line. From the data shown in Fig. 5, note that the power delivery schemes with both DSDG and SSSG perform better than the power grid with DSSG. The power distribution grid with DSDG outperforms the reference power grid by 0.7%. This behavior can be explained as follows. Since the number of lines dedicated to each power delivery network in the grid with DSDG is two times smaller than the total number of lines in the reference grid, the resistance of each subnetwork is two times greater than the resistance of the reference power grid. The loop inductance of an interdigitated power distribution grid depends inversely linearly on the number of lines in the grid [12]. The loop inductance of each subnetwork is two times larger than the overall loop inductance of the grid with SSSG. Given two similar current loads applied to the reference power distribution scheme, the maximum voltage drop for both systems should be the same. However, from (3), the mutual inductive coupling in the power grid with DSDG increases due to the presence of the second subnetwork. As a result, the overall loop inductance of each network comprising the power grid with DSDG is lower, resulting in lower power noise as seen from the current load of each subnetwork. In many applications such as high performance microprocessors, mixed-signal circuits, and systems-on-chip, a power distribution network with DSDG is often utilized. In other applications, however, a power distribution system with multiple voltages and multiple grounds can be an alternative to power distribution systems with SSSG.

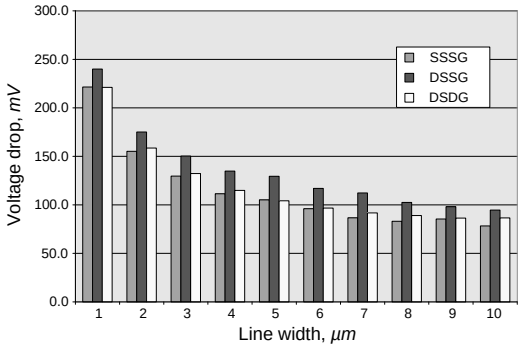
4.2 Power Distribution Grids with Decoupling Capacitors

To lower the voltage fluctuations of on-chip power delivery systems, decoupling capacitors are placed on ICs to provide charge when the voltage drops [4]. The maximum voltage drop of three power distribution schemes with different amounts of decoupling capacitances is shown in Fig. 6. All of the decoupling capacitors are assumed to be ideal, *i.e.*, without any parasitic resistances and inductances associated with the capacitor. The total budgeted capacitance is divided equally between the two supply voltages. The decoupling capacitor added to the power distribution grid with SSSG is two times larger than the decoupling capacitor in each subnetwork of the power delivery scheme with dual voltages. As shown in Fig. 6, the maximum voltage drop decreases as the lines become wider. The maximum voltage drop of the proposed power distribution scheme with DSDG is reduced by 13.3% on average (19.5% maximum) and 18% on average (32.3% maximum) for 20 pF and 30 pF decoupling capacitances, respectively, as compared to a conventional power distribution scheme with DSSG.

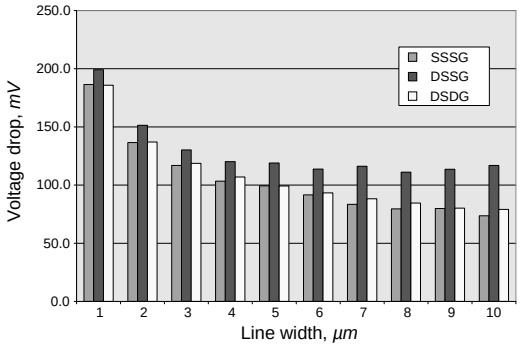
Comparing Fig. 5 to Fig. 6, note that the voltage drop of the power distribution grids with decoupling capacitors, as compared to the case with no decoupling capacitances, is greatly reduced for narrow lines and is higher for wider lines. This phenomenon can be explained as follows. For narrow lines, the grid resistance is high and the loop inductance is low. The grid impedance, therefore, is primarily determined by the resistance of the lines. Initially, the system with an added decoupling capacitor is overdamped. As the lines become wider, the grid resistance decreases faster than the increase in the loop inductance and the system becomes less damped. As the loop inductance increases, the resonant frequency of an RLC circuit, formed by the on-chip decoupling capacitor and the parasitic RL impedance of the grid, decreases. This resonant frequency moves closer to the switching frequency of the current load. As a result, the voltage response of the overall system oscillates. Since the decoupling capacitance added to the power grid with SSSG is two times larger than the decoupling capacitance added to each power supply voltage in the dual voltage schemes, the system with a single supply voltage is more highly damped and the self-resonant frequency is significantly lower. Moreover, the resonant frequency is located far from the switching frequency of the circuit. For most line widths at 1 GHz, the resulting power noise in the power grid with DSDG is greater than the power noise of the power distribution scheme with SSSG, as shown in Fig. 6(a).

Increasing the on-chip decoupling capacitance from 20 pF to 30 pF further reduces the voltage drop below the power supply level. For a 30 pF decoupling capacitance in a power delivery scheme with DSSG, the self-resonant frequency is close to the switching frequency of the current load. Simultaneously, the grid resistance decreases much faster with increasing line width than the increase in the loop inductance. The system becomes underdamped with a self-resonant frequency equal to the circuit switching frequency. As a result, the system produces high amplitude voltage fluctuations. Therefore, the maximum voltage drop in the case of a power

grid with DSSG increases as the lines become wider. This phenomenon is illustrated in Fig. 6(b) for line widths of 7 μm and wider.



(a) Decoupling capacitance budget of 20 pF



(b) Decoupling capacitance budget of 30 pF

Figure 6: Maximum voltage drop for three types of power distribution grids with a decoupling capacitance of (a) 20 pF and (b) 30 pF added to each power supply.

With decoupling capacitors, the self-resonant frequency of an on-chip power distribution system is lowered. If the resonant frequency of an *RLC* system with intentionally added decoupling capacitors is sufficiently close to the circuit switching frequency, the system will produce high amplitude voltage fluctuations. Voltage sagging below the power supply level will degrade system performance and may cause significant failure. An improper choice of on-chip decoupling capacitors can therefore worsen the power noise, further degrading system performance [13,14].

4.3 Dependence of Power Noise on Switching Frequency of Current Loads

To model the dependence of the power noise on the switching frequency, the power grids are stimulated with triangular current sources with 50 mA amplitude, 20 ps rise times, and 30 ps fall times. The switching frequency of each current source varies from 1 GHz to 10 GHz to capture resonances in each power grid. For each grid structure, the width of the line is varied from 1 μm to 10 μm. The maximum voltage drop from V_{dd} is estimated from SPICE for different line widths at each frequency.

The maximum voltage drop below the power supply level for the power distribution grid with SSSG is illustrated in Fig. 7. The maximum voltage drop decreases slightly for wider lines. Note that with decoupling capacitors, the voltage drop is lower except for two regions. The significant increase in power noise at specific frequencies and line widths is due to the following reasons. As lines become wider, the resistance of the power grid is lower, whereas the inductance is slightly increased, decreasing the damping of the entire system. When the switching frequency of a current load approaches the self resonant frequency of the power grid, the voltage drop caused by the *RLC* system increases. This phenomenon is known as resonance. As the width of the lines increases, the system becomes more underdamped, resulting in a sharper resonant peak. The amplitude of the resonant peak increases rapidly as the system becomes less damped. The maximum voltage drop occurs between 6 GHz and 7 GHz for a power grid with a 20 pF decoupling capacitance, as shown in Fig. 7(a).

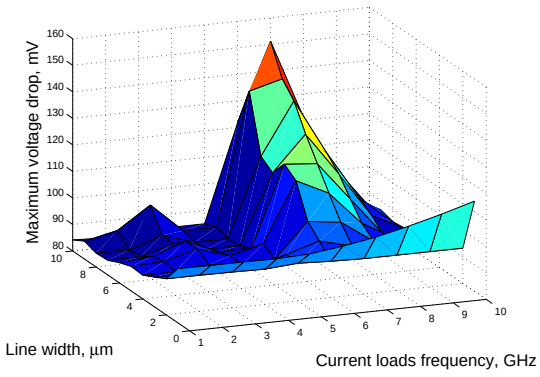
Another increase in the maximum voltage drop occurs at high frequencies in narrow lines. Decoupling capacitors are effective only if the capacitor is fully charged within one clock cycle. The effectiveness of the decoupling capacitor is related to the *RC* time constant, where R is the resistance of the interconnect connecting the capacitor to the load. For narrow resistive lines, the time constant is prohibitively large at high frequencies, *i.e*, the capacitor cannot be fully charged within one clock period. The effective magnitude of the decoupling capacitor is therefore reduced. Thus, the capacitor has the same effect on the power noise as a smaller capacitor.

By increasing the magnitude of the decoupling capacitor, the overall power noise can be further reduced, as shown in Fig. 7(b). Moreover, the system becomes more damped, producing a resonant peak with a smaller amplitude. The self resonant frequency of the power delivery system is also lowered. Comparing Figs. 7(a) to 7(b), note that the resonant peak shifts in frequency from approximately 6 GHz to 7 GHz for a 20 pF decoupling capacitance to 5 GHz to 6 GHz for a 30 pF decoupling capacitance. Concurrently, increasing the decoupling capacitor increases the *RC* time constant, making the capacitor less effective at high frequencies in narrow resistive lines. Note the significant increase in the maximum voltage drop for a 1 μm wide line for a 30 pF decoupling capacitance as compared to the case of a 20 pF decoupling capacitance. Power distribution grids with DSSG and DSDG behave similarly. For the same decoupling capacitance, the power distribution scheme with DSDG results in a lower voltage drop than a power distribution scheme with DSSG. The value of decoupling capacitance needs to be carefully chosen to guarantee that the two prohibited regions are outside the operating frequency of the system for a given line width. Alternatively, for narrow lines, the magnitude of the decoupling capacitor is limited by the *RC* time constant. The amplitude of the resonant peak can be lowered by increasing the parasitic resistance of the decoupling capacitors.

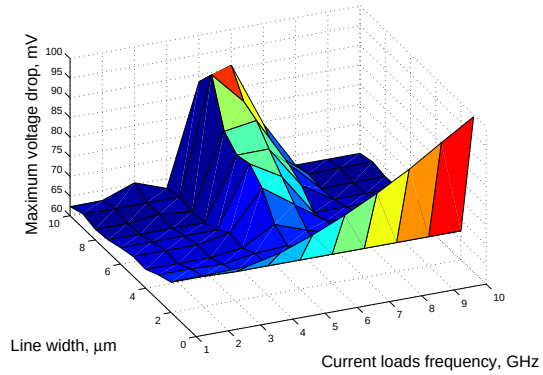
5. CONCLUSIONS

Power distribution grids with multiple power supply voltages are analyzed in this paper. An on-chip power distribu-

tion system with DSDG is proposed. It is shown that in the case of no decoupling capacitors placed between the power supply and ground, the proposed power delivery scheme outperforms by about a 17% reduction in power noise as compared to a conventional power distribution system with DSSG. In the case of power grids with decoupling capacitors, the voltage drop is reduced to about 13% and 18% for 20 pF and 30 pF decoupling capacitors, respectively.



(a) Decoupling capacitance budget of 20 pF



(b) Decoupling capacitance budget of 30 pF

Figure 7: Maximum voltage drop for power distribution grid with SSSG as a function of frequency and line width for different values of decoupling capacitance.

The performance of the proposed on-chip power distribution scheme is compared to a reference power distribution grid with SSSG. If no decoupling capacitors are added, the voltage drop of a power distribution grid with DSDG is slightly reduced as compared to the voltage drop of a SSSG power distribution system. On-chip decoupling capacitors lower the self-resonant frequency of the on-chip power distribution grid which can produce resonances. The system of decoupling capacitors in power distribution systems with multiple supply voltages therefore requires careful design. Improper choice of on-chip decoupling capacitors can further degrade the performance of a system.

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