Timing Optimization of Interconnect by Simultaneous Net-Ordering, Wire Sizing and Spacing

Konstantin Moiseev
Electrical Engineering Dept.
Technion
Haifa 32000, Israel
mkostya@tx.technion.ac.il

Shmuel Wimer
Intel Israel (74) Ltd.
Mobile Platform Group
Haifa 31015, Israel
Shmuel.wimer@intel.com

Avinoam Kolodny
Electrical Engineering Dept.
Technion
Haifa 32000, Israel
kolodny@ee.technion.ac.il

Abstract – **This paper addresses the problem of ordering and sizing parallel wires in a single metal layer within an interconnect channel of a given width, such that cross-capacitances are optimally shared for circuit timing optimization. Using an Elmore delay model including cross capacitances for a bundle of wires, we show that an optimal wire ordering is uniquely determined, such that best timing can be obtained by proper allocation of wire widths and inter-wire spaces. The optimal order, called BMI (Balanced Monotonic Interleaved) depends only on the size of drivers for a wide range of cases. Heuristics are presented for simultaneous ordering, sizing and spacing of wires. Examples for 90-nanometer technology are analyzed and discussed.**

1. INTRODUCTION

Cross-capacitances between wires in interconnect structures have a major effect on circuit timing. Allocation of inter-wire spaces and wire widths is an optimization problem for interconnect structures under a total area constraint [1]. This paper addresses a more general problem, where delays in a bundle of parallel nets (with different drivers and loads) are minimized by choosing an *optimal ordering of the nets*, in addition to optimal allocation of wire widths and inter-wire spaces. The total width of the structure is a given constraint. The problem is motivated by the following example: Two different arrangements of the same wires, presented in Fig.1 a and Fig.1 b result in different circuit timing. In the second case inter-wire spaces are shared more effectively due to grouping of wires of each driver type together. A brute-force approach to determine the best ordering is to generate all signal permutations, and solve the wire-width and space optimization problem for each permutation. This approach is computationally infeasible for practical channels. The existence of an optimal wire ordering that yields best delay minimization after wire sizing and space allocation is proven in this paper. An efficient algorithm to find the optimal order for a wide range of practical cases is described. Heuristics for solving the more general cases of this problem are evaluated.

The problem of allocating widths and spaces to maximize performance in tuning of bus structures was proposed in [1]. The wire sizing problem has been addressed in [2] and [3] for a single net. Sizing and spacing multiple nets with consideration of coupling capacitance has been addressed in [4] for general interconnect layouts by converting cross capacitance to effective fringe capacitance, and for bus structures in [22]. Coupling capacitance has been addressed explicitly in the context of physical design for minimizing crosstalk noise [5,6] or dynamic power [7]. Some authors treated the problem of throughput optimization in buses using uniform wire widths and spaces [21, 23,24]. Several variants of net-reordering have been applied for improving layout efficiency [8], and for noise reduction [6, 9, 10, 11, 12]. Swapping of wires for power reduction was applied in [13]. Vittal et al. [11] have suggested without proof to reduce capacitive coupling noise by sorting wires in order of driver strength, which is closely related to our results. However, delay optimization by net-ordering has not been addressed in previous works.

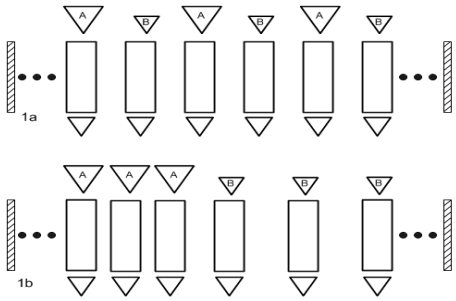

Figure 1. Two ways to order wires in an interconnect channel. *"A" – strong drivers (small resistance), "B" – weak drivers (large resistance). Case a: interleaved placement, all wires share equal spaces. Case b: sorted placement, wires with weak drivers share large spaces and wires with strong drivers share small spaces, with improved circuit timing.*

2. PROBLEM FORMULATION

Circuit structure and notation are shown in Figure 2, illustrating n signal nets $\sigma_0,\ldots,\sigma_{n-1}$ between two shield wires. S_i and S_{i+1}, respectively, denote spaces to the left and right neighbors of wire σ_i. W_i is the wire width. The length of all the wires is L. The total sum of wire widths and spaces is constrained to be A, representing the area available for laying out all of the signal wires.

$$g(\overline{W},\overline{S}) = \sum_{j=0}^{n-1} W_j + \sum_{j=0}^{n} S_j = A \qquad (2.1)$$

This is a common structure, which is amenable to simple mathematical analysis. Wires with repeaters can be segmented into several problem instances of this form. The delay Δ_i of signal σ_i can be calculated from the π-model equivalent circuit shown in Figure 3, where R_i is the effective output resistance of the driver, R_{w_i} is the wire resistance, C_{w_i} is the area and fringe capacitance, C_{c_i} and $C_{c_{i+1}}$ are the coupling capacitances to the

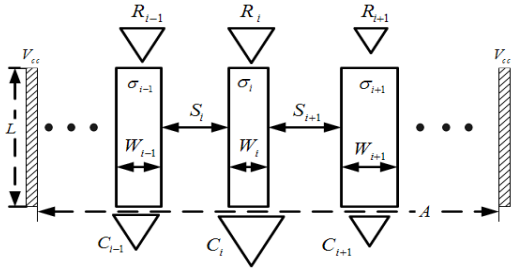

Figure 2. Interconnect configuration. *The total channel width is A and the length is L. Each wire* σ_i *is of width* W_i*, with spaces to neighbors* S_i *and* S_{i+1}*, driven by a gate with effective resistance* R_i *and loaded by a gate with capacitance* C_i *.*

right and left neighboring signals, and C_i is the capacitive load of the receiver's input.

Using an Elmore model with first order approximation for capacitances [19], the delay can be expressed as [18]:

$$\Delta_i = (a + \frac{b}{W_i} + \frac{dm_{i-1,i}}{W_i S_i} + \frac{dm_{i,i+1}}{W_i S_{i+1}} + \frac{eC_i}{W_i} + kR_i W_i + gR_i + \frac{hR_i m_{i-1,i}}{S_i} + \frac{hR_i m_{i,i+1}}{S_{i+1}} + R_i C_i) \quad (2.2)$$

where coefficients of wire widths, spaces, driver resistances and load capacitances are technology-dependent constants and $m_{i,j}$ is Miller factor between wires i and j. If all wires can switch simultaneously, the cross-capacitance terms are typically multiplied by a uniform $m_{i,j}$ of 2. For this worst-case assumption, inter-wire tradeoffs become very significant in optimizing the layout. For nominal delays, $m_{i,j} = 1$ is assumed. Derivations in this paper use this assumption. Despite its simplicity, this Elmore-based modeling approach is widely used in practical interconnect optimizations. With empirical parameter tuning, the model accuracy can be improved further. In [18], good absolute accuracy versus circuit simulation has been obtained. Interesting tradeoffs can be made because wire resistance and capacitance change in opposite directions as wire width grows, and increased spacing reduces the side-capacitance shared by adjacent wires. Hence, wire reordering can change adjacency relations and affect the optimal allocation of spaces and wire widths.

Let f_1 given in (2.3) be the objective function we wish to minimize. f_1 denotes the sum of all signal delays. It is commonly used in early design stages since it captures the contributions of all signals to circuit timing.

$$f_1 = \sum_{i=0}^{n-1} (a + \frac{b}{W_i} + \frac{d}{W_i S_i} + \frac{d}{W_i S_{i+1}} + \frac{eC_i}{W_i} + kR_i W_i + gR_i + \frac{hR_i}{S_i} + \frac{hR_i}{S_{i+1}} + R_i C_i) \quad (2.3)$$

For final performance tuning, it is appropriate to speed-up the slowest signal. The objective function for such MinMax optimization is

$$f_2 = \max_{0 \le i \le n-1} \left\{ (a + \frac{b}{W_i} + \frac{d}{W_i S_i} + \frac{d}{W_i S_{i+1}} + \frac{eC_i}{W_i} + kR_i W_i + gR_i + \frac{hR_i}{S_i} + \frac{hR_i}{S_{i+1}} + R_i C_i) \right\} \quad (2.4)$$

When required times of signals are specified, the corresponding objective functions are sum of slacks and the worst slack among all signals. Minimizing the sum of slacks is equivalent to minimizing f_1. The case of minimizing worst slack can be transformed to minimizing worst wire delay f_2.

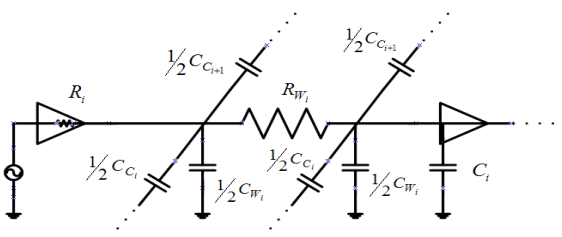

Figure 3*. Equivalent circuit for calculating the* i^{th} *signal delay*

3. SUM OF DELAYS OPTIMIZATION

Let each wire have width W_i assigned as follows:

$$W_i = \frac{1}{\psi(R_i)}, \quad (3.1)$$

where ψ **is a monotonically non-decreasing** functions of driver resistance R_i. Such assignment is practically common, as one attempts to balance the resistance of the driver and the resistance of the driven line and is known as "impedance matching". Notice that the case of uniform width wires is also covered by (3.1). f_1 is a function of $n+1$ variables S_i. The solution of minimizing f_1 under the constraint g (in (2.1)) implies

$$\frac{\partial f_1}{\partial S_j} + \lambda \frac{\partial g}{\partial S_j} = 0, \; 0 \le j \le n \quad (3.2)$$

where λ is a Lagrange multiplier. Taking partial derivatives of f_1 and g with respect to S_i, substituting to (3.2) and rearranging we obtain

$$S_0^2 + S_2^2 + S_4^2 + \quad + S_{n-1}^2 = S_1^2 + S_3^2 + S_5^2 + \quad + S_n^2 \quad (3.3)$$

Notice that (3.3) holds regardless of wire widths, reflecting the fact that adjacent wires share common spaces. Equations (3.2) can be solved for S_i and λ. By substitution to (2.3), the minimal total sum of delays is expressed in terms of technology parameters, total area constraint and wire driver resistances:

$$f_1 = na + b\sum_{i=0}^{n-1}\psi(R_i) + k\sum_{i=0}^{n-1}\frac{R_i}{\psi(R_i)} + g\sum_{i=0}^{n-1}R_i + e\sum_{i=0}^{n-1}\psi(R_i)C_i + \sum_{i=0}^{n-1}C_i R_i + \quad (3.4)$$
$$+ \frac{1}{A - \sum_{i=0}^{n-1} W_i}\left(\sum_{i=0}^{n-2}\sqrt{(d\psi(R_i) + d\psi(R_{i+1}) + hR_i + hR_{i+1})} + \right.$$
$$\left. + \sqrt{d\psi(R_0) + hR_0} + \sqrt{d\psi(R_{n-1}) + hR_{n-1}} \right)^2$$

The quadratic last term of (3.4) depends on wire ordering. Consequently, there exists an order which minimizes the total sum of delays. The important conclusion from expression (3.4) is that ***for wire widths assigned as in (3.1), wire ordering affects the minimal sum of delays via driver resistances, while the effect of load capacitances is order-insensitive.***

We now describe how to obtain the optimal order. The driver with the largest resistance is taken to reside at the center of the channel. The other drivers are taken in monotonically decreasing order of driver resistance, and located alternately on the left and right of as shown in figure 4. We call the resulting order BMI (Balanced Monotonic Interleaved). The advantage of BMI order stems from the fact that spaces are shared by wires with similar driver resistances, since the side-capacitance to the sidewalls can be modeled as capacitance to ground, hence the sidewalls affect our model as if they were wires with zero-resistance drivers.

Definition (BMI order): Given a channel of n signals with driver resistances $R_0, \ldots, R_{n-1}$, the permutation of signals $\Pi^* = (R_0, \ldots, R_{n-1})$ is called *Balanced Monotonic Interleaved* (BMI) if it satisfies

$$R_0 < R_{n-1} < R_1 < R_{n-2} < \quad < R_{\left\lceil \frac{n}{2} \right\rceil - 1} < R_{\left\lceil \frac{n}{2} \right\rceil + 1} < R_{\left\lceil \frac{n}{2} \right\rceil}. \quad (3.5)$$

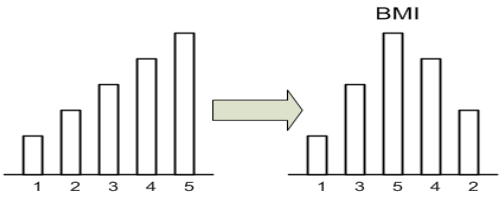

***Figure 4**. Building BMI order from a set of wires sorted according to driver resistance*

Notice that the reversed permutation which satisfies $R_{n-1} < R_0 < R_{n-2} < R_1 <$, is also BMI.

Theorem 1 (Optimal order): Let wire width be a monotonic non-increasing function of driver resistance. The net-ordering yielding minimal sum of delays is then BMI.

The function $\psi(R)$ (3.1) needs to be selected carefully. Although the theorem holds for equal-width wires, the goal is to approach the absolute minimum which could be achieved in the space of all orderings, wire width and wire spacing assignments. A simple, yet practical, wire width function is the inverse linear

$$W_i(R_i) = \frac{\alpha}{\beta + \gamma R_i}, \qquad (3.6)$$

where α , β and γ are positive constants. In the most general case, both wire widths and spaces can vary arbitrarily, yielding $2n+1$ equations. In this case the optimal wire ordering may depend on the values of capacitive loads and is not necessarily BMI. The next theorem defines conditions for optimality of BMI order in the most general case.

Theorem 2: For a given set of n wires, if each pair of wires σ_i and σ_j with driver resistances and load capacitances (R_i , C_i) and (R_j , C_j) satisfy $R_i > R_j$ and $C_i \le C_j$, then the optimal order of this set of wires is BMI, under total sum of wire delays objective function.

If the conditions of the theorem are not met, the solution of the most general problem is very complex, as it involves the exploration of many permutations.

In order to make the computational effort reasonable, the following heuristic is proposed. It is based on the BMI order and yields near-optimal solutions. The complex optimization problem is divided into two successive simpler ones. First, theorem 2 is checked. If it is satisfied, the optimal order is BMI. Otherwise, the heuristic assigns wire widths by some parameterized monotonic non-increasing function such as (3.6). BMI order is now guaranteed to be optimal. Then continuous optimization is applied, exploring for the optimal values of inter-wire spaces and the width-function parameters (e.g. α , β and γ in (3.6)). This heuristic reduces time complexity of the optimization problem by factor of $O(n!)$ and reduces the number of unknown parameters from $2n+1$ to $n+p$, where p is the number of parameters in the width function. Experiments show that a well-chosen width-function yields ordering, widths and spaces that result in total sum of delays which is very close to the global optimum.

4. OPTIMAL ORDERING OF WIRES UNDER MAXIMUM DELAY OBJECTIVE

In this section, we examine ordering optimization for minimizing worst wire delay (2.4). We aim to demonstrate optimality of BMI order for minimization of worst wire delay as well. However, since (2.4) is not differentiable, the technique used for deriving optimal order for total sum of delays cannot be applied here. We have demonstrated experimentally that BMI order is optimal under maximum delay objective in most cases. We have created about 1000 random problem instances for 5 wires and 100 random problem instances for 6 wires and obtained BMI optimal order in most cases (the computational effort is infeasible for a larger number of wires). We have found that when load capacitances are not all equal, in about 80% of cases the optimal order is BMI. When all load capacitances are equal, the relative number of optimal BMI orders rises to 93-95%. We have found that with equal capacitances, the cases which deviated from BMI (7-5 %) were caused by effects of proximity to the shield wires at the sides, since spaces to the shield wires are not shared by a pair of signals. These effects become significant only if driver resistances are nearly equal.

5. RESULTS AND DISCUSSION

Numerical experiments for various problem instances were performed using 90 nanometer technology parameters calculated based on [15]. We have simulated some circuits in Spice before and after optimization, to verify the delay improvement. In the first experiment we evaluated 20 random problem instances using five signals. Each signal was assigned a driver randomly. The range of driver resistances was 100 Ω to 2 $K\Omega$ and load capacitances in the range 200 fF to 10 fF were assigned accordingly, to avoid excessive driver loading, such that the conditions of theorem 2 are always satisfied. For each problem the wire widths and spaces were optimized to yield minimum total sum of delays and minimum worst wire delay. This was done for all the 5!=120 possible order permutations. The procedure was repeated for five different channel widths A – 5, 10, 15, 20 and 25 μm , and five different lengths L – 300, 500, 1000, 5000 and 10000 μm . The optimization impact (% improvement of best versus worst ordering, after width/space optimization, averaged for 20 random problem instances) is presented in Table 1. In each cell, the upper half cell (colored in gray) represents total sum of delays optimization and the lower half cell – worst wire delay optimization. Worst case crosstalk was assumed (i.e. Miller factor of 2). This experiment demonstrates that net ordering can significantly improve results of wire sizing and spacing optimization. The worst wire delay objective is affected more than sum of delays. Since theorem 2 is always satisfied in this example, all obtained optimal orders for total sum of delays minimization are BMI. On the other hand, only 80% of the obtained optimal orders for minimization of worst delay are BMI.

Table 1
Average improvement (best vs. worst ordering) for random problem instances, in sum-of-delays (upper halfcell) and worst wire delay (lower halfcell)

	A=5 µm	A=10 µm	A=15 µm	A=20 µm	A=25 µm
L=300 µm	*7.14%*	*6.13%*	*5.13%*	*4.25%*	*3.62%*
	18.60%	13.23%	9.89%	7.68%	6.14%
L = 500 µm	*8.41%*	*7.39%*	*6.31%*	*5.40%*	*4.71%*
	20.73%	16.17%	12.91%	10.56%	8.79%
L = 1000 µm	*9.51%*	*8.57%*	*7.65%*	*6.71%*	*5.97%*
	22.14%	18.83%	16.05%	13.82%	12.03%
L = 5000 µm	*9.65%*	*8.67%*	*7.97%*	*7.24%*	*6.63%*
	20.64%	19.41%	17.75%	16.19%	14.79%
L =10000 µm	*8.62%*	*7.91%*	*7.29%*	*6.59%*	*5.99%*
	18.61%	18.05%	16.71%	15.37%	14.14%

The second example shows in Table 2 the effect of signal ordering on wires with both strong and weak drivers. A channel of 7 signals with driver – load pairs of (100 Ω – 50 fF) or (1.9 $K\Omega$ – 5 fF) was examined for various numbers of the weak drivers. Bus width and length were A=12 μm and L=600 μm . As could be expected, when the numbers of strong and weak drivers were about equal, signal ordering was most effective. The worst ordering was indeed the interleaved one described in Figure 1a, while the best one was clearly BMI. Miller factor of 1 was assumed (nominal delays).

Table 2

% improvement of best versus worst ordering, after width/space optimization, for a bus with two driver strengths

No. of weak drivers	Worst delay optimization	Sum of delays optimization
1	0.17%	0.39%
2	8.94%	4.81%
3	13.81%	8.12%
4	18.17%	11.19%
5	11.99%	7.52%
6	6.16%	3.55%

In the third example, delays obtained by exhaustive simultaneous ordering/sizing/spacing optimization are compared with results of heuristics using BMI order for total sum of delays objective. We used the same set of 20 instances as in example 1. The heuristic described in section 3 with the inverse linear width function (eq. 3.6) was applied. The results are presented in Table 3. For each value of bus width and length, the delay interval between the optimal result of exhaustive search and the optimal result of the heuristic is presented as a fraction of the delay interval between best and worst results of the exhaustive search. As can be seen, by using parametric width optimization, the global minimum was approached as closely as 0.37% on average.

Table 3

Relative delay distance of heuristic result to global minimum

	A=5	A=10	A=15	A=20	A=25
L=300	0.16%	0.14%	0.42%	0.19%	1.34%
L = 500	0.20%	0.25%	0.15%	0.18%	0.29%
L = 1000	0.13%	0.14%	0.19%	0.28%	0.35%
L = 5000	0.17%	0.21%	0.28%	0.45%	0.65%
L =10000	0.25%	0.28%	0.38%	0.52%	0.66%
Average	*0.182%*	*0.204%*	*0.284%*	*0.324%*	*0.658%*

6. CONCLUSION

We have shown that reordering of wires can improve results of timing optimization by wire-sizing and spacing, for a wiring channel of constrained width. The optimal order of wires generally depends on both wire driver resistances and load capacitances. Analysis of sum-of-delays minimization showed that when wire widths are uniform or are specified by a monotonic non-increasing function of driver resistance, the optimal order can be determined directly. This optimal order is BMI (Balanced Monotonic Interleaved) and depends on driver resistances only. Load capacitances do not affect the optimal order under these conditions. The general problem of simultaneous net-ordering, wire-sizing and spacing optimization has been presented. In the general case, the optimal solution might be dominated by load capacitances, and the optimal order may not be BMI. Solution heuristics were proposed for the general case. Numerical experiments demonstrated heuristic results approaching the global optimum within approximately 0.5%.

REFERENCES

1. A. Kahng, S. Muddu, E. Sarto and R. Sharma, "Interconnect Tuning Strategies for High-Performance ICs", *Proc. Design, Automation and Testing in Europe*, pp. 471-478, Feb. 1998.
2. J. Cong and K. Leung, "Optimal Wiresizing Under Elmore Delay Model". *IEEE Trans. on Computer-Aided Design*, vol. 14, no. 3, pp. 321-336, Mar. 1995.
3. S. Sapatnekar, "Wire Sizing as a Convex Optimization Problem: Exploring the Area Delay Tradeoff*", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 8, pp. 1001-1011, Aug. 1996.
4. J. Cong, L. He, C. Koh and Z. Pan, "Interconnect Sizing and Spacing with Consideration of Coupling Capacitance", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,* vol. 20, no. 9, pp.1164 -1169, Sep. 2001.
5. M. Becer, D. Blaauw, V. Zolotov, R. Panda and I. Hajj, "Analysis of Noise Avoidance Techniques in Deep-Submicron Interconnects Using a Complete Crosstalk Noise Model", *IEEE/ACM Design Automation and Test in Europe Conference (DATE)*, pp. 456-463, Mar. 2002
6. D. Kirkpatrick and A. Sangiovanni-Vincentelli. "Techniques for crosstalk avoidance in the physical design of high performance digital systems", *In Proc. IEEE/ACM Int. Conf. Computer Aided Design*, pp. 616-619, Nov. 1994.
7. R. Arunachalam, E. Acar, and S. Nassif, "Optimal shielding/spacing metrics for low power design", *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, pp. 167-172, 2003.
8. P. Groeneveld, "Wire ordering for detailed routing", *IEEE Design and Test*, vol.6, issue 6, pp. 6-17, Nov. 1989.
9. A.Vittal, L Chen, M. Marek-Sadowska, K. Wang, S Yang, "Crosstalk in VLSI Interconnections", *IEEE Transactions on CAD Design of IC and Systems*, Vol.18, No. 12, Dec. 1999.
10. T. Gao and C. Liu, "Minimum Crosstalk Channel Routing", *TechnicalDigest Int. Conf. on CAD*, pp. 692-696, 1993.
11. J. Ma and L. He, "Formulae and Applications of Interconnect Estimation Considering Shield Insertion and Net Ordering", *2001 International Conference on Computer-Aided Design (ICCAD '01)*, pp. 327-332, Nov. 2001.
12. P. Gupta and A. Kahng. "Wire Swizzling to Reduce Delay Uncertainty Due to Capacitive Coupling." *Proc. IEEE Intl. Conf. on VLSI Design*, January, p.431, 2004.
13. E. Macii, M. Poncino and S. Salerno, "Combining Wire Swapping and Spacing for Low-Power Deep-Submicron Buses", *Proc.of the 13th ACM Great Lakes symposium on VLSI*, pp. 198-202*,* 2003.
14. D. Kirkpatrick and A. Sangiovanni-Vincentelli, "Digital Sensitivity: Predicting Signal Interaction using Functional Analysis", *Proc.IEEE/ACM International Conference on Computer Aided Design,* pp. 536-541, 1996.
15. Berkeley Predictive Technology Model, http://www-device.eecs.berkeley.edu/~ptm/.
16. T. Sato, Y. Cao, D. Sylvester and C. Hu, "Characterization of interconnect coupling noise using in-situ delay change curve measurements", *Proc. IEEE ASIC/SoC Conf.*, pp. 321-325, 2000.
17. P. Chen and K. Keutzer, "Toward true crosstalk noise analysis", *Proc. ICCAD*, pp. 132-137, 1999.
18. A. Abou-Seido, B. Nowak and C. Chu, " Fitted Elmore Delay: A Simple and Accurate Interconnect Delay Model*", IEEE Transactions on VLSI Systems*, vol. 12, no. 7, pp. 691-696, July 2004.
19. S. Wong, G. Lee and D. Ma, "Modeling if Interconnect, Capacitance, Delay and Crosstalk in VLSI", *IEEE Transactions on Semiconductor Manufacturing*, vol. 13, no.1, pp. 108-111 Feb. 2000.
20. T. Sato, Y. Cao, K. Agarwal, D. Sylvester and C. Hu, "Bidirectional Closed-Form Transformation Between On-Chip Coupling Noise Waveforms and Interconnect Delay-Chamge Curves", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol.22, no.5, pp. 560-572, May 2003.
21. T. Lin and L. Pillegi, "Throughput driven IC Communication Fabric Synthesis", *Proc. ICCAD*, pp. 274-279, 2002.
22. S. Michaely, S. Wimer and A. Kolodny, "Optimal resizing of bus wires in layout migration", *Proc. ICECS 2004*, pp. 411-414, 2004.
23. A. Naeemi, R. Venkatesan, and J. D. Meindl, "Optimal global interconnects for GSI," *IEEE Trans. Electron. Devices*, vol. 50, pp. 980-987, April 2003.
24. D. Pamunuwa, L. Zheng and H. Tenhunen, "Maximizing throughput over parallel wire structures in the deep submicrometer regime", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Volume 11 Issue 2, 2003.