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Power Grid Analysis Based on a Macro Circuit Model

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Abstract—Analysis and design of on-chip power grids are complex problems. A typical grid consists of hundreds of millions of transistors that act as current consumers. Typical algorithms for power grid analysis or power grid automatic design, model the current consumers, namely the CMOS logic gates, as ideal current sources. In this study we offer a new methodology for modeling the power-consuming gates on the grid. Our approach is based on the analysis of the total dissipated power by these consumers. We propose a new model for the current consumers, based on effective impedance. In this model, only passive elements are employed. It relies on a calculation of the effective capacitance and effective resistance of the logic gates. Since during each clock period the dissipated power and the stored energy are exactly represented, total energy and power are exactly modeled. Methods from statistical/computational physics can be adopted to represent clusters of consumers on each sub-grid as "macro-circuits". The interaction between the power grid and the current consumers is taken into account in this model and an example for it is presented.

I. INTRODUCTION

The design of an efficient power distribution grid in integrated circuits is one of the key challenges in VLSI design. The complexity of power grids raises the need for simple models for the devices in the grid and time-efficient algorithms for the analysis and design of the grid.

A. The Challenges in Power Distribution Networks

As technology developed, the power requirements in integrated circuits are rising – the current demand increases, as well as the power density [1]. The interconnect in the power grid is modeled as a network of resistors and inductors. Because of the resistance and inductance throughout the grid, there is a voltage drop between the supply voltage and the logic gates. The voltage drop can be classified as IR-drop or LdI/dt drop due to the parasitic resistance and the parasitic inductance respectively [2].

The voltage drop is an undesirable phenomenon, it slows the circuit and therefore the performance and functionality of the integrated circuit are compromised. If the voltage drop is excessive, it can cause logic errors. Therefore, the grid should be designed to have a low voltage drop in all of the nodes.

In order to lower the fluctuations in the supply voltage, decoupling capacitors are connected between nodes in the voltage supply grid and ground grid throughout the network. The decoupling capacitors store electric charge and supply the charge in case of fluctuations in the voltage and in this manner they reduce the fluctuations. The basic schematic for a power grid is shown in Figure 1 (a).

B. Current Consumer Conventional Model

Modern integrated circuits can contain billions of transistors [3]. Those transistors are the components of logic gates, which act as the current consumers of the power grid. While switching, every logic gate consumes current from the power supply throughout the grid. Since transistors are non-linear devices, the conventional method for modeling the transistors is to simulate individual circuit blocks, including transistors and parasitic elements in the power interconnect, and then replace each block by an ideal current source. The current waveforms assigned to these sources serve as excitation sources for the grid. This way the analysis problem becomes linear [2], [4]. The basic schematic for this model is shown in Figure 1 (b).

Although this model is quite intuitive, the use of this model is still complex and simulations with this model take unreasonable time because of the large size of the network and the large numbers of current sources [5]. Furthermore, the ideal current source model has several deficiencies. It is somewhat inappropriate to take an active supply which adds energy to the system and use it as a model for a consumer of power which actually dissipates energy from the power supply. The ideal current source model ignores the interaction between the logic gates and the power grid, such as the changes in the consumed current due to supply voltage drop.

In order to estimate the current of the ideal current source several methods have been developed. One approach is to model the current as a random variable and use stochastic methods [5]. Other approaches model the current as an average DC current and a peak current by simplifying the model to a triangular and trapezoidal current waveforms [7]. Since the estimation of the current is simplified and inaccurate, those models produce a significant error in the power grid analysis [8]. Therefore, a simple model which is accurate for large circuits, based on passive elements, would be useful.

The remainder of the paper is organized as follows. In section II the basic current consumer model (*i.e.* microcircuit) and the sub grid problem definition (*i.e.* macro circuit) are described. In Section III an example for the interaction between the power grid and the current consumer is presented. In section IV the deviations from the model being discussed and Section V contains a summary of the paper.

II. MICRO AND MACRO CIRCUITS

In this model each current consumer is represented as a microcircuit and a cluster of microcircuits is represented as a single simple macro circuit.

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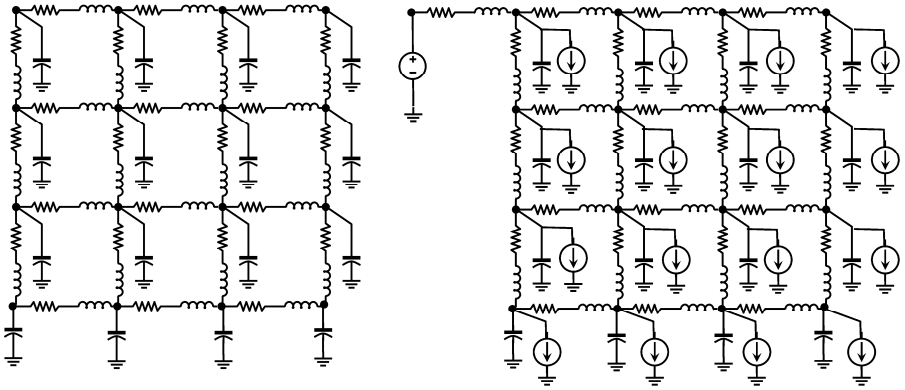


Figure 1. (a) An RLC model of an on-chip power distribution network [11]. (b) A full RLC and conventional current consumer model as ideal current source [5].

A. Model Concept

Individual logic switching events do not affect the power supply behavior since the power supply provides current to numerous current consumers and many decoupling capacitors, which supply charge to the nearby current consumers, spread all over the grid and averaging the supplied current. Therefore the changes in the behavior of the power supply are much slower in comparison with the clock (which affects single switching elements).

The model is based on taking the current consumer behavior parameters from the integrated circuit clock time scale (typically picoseconds or nanoseconds) [6] and transferring those parameters to the power supply time scale (typically microseconds or milliseconds) [2], without losing correctness because of energy and power conservation in the model.

Each current consumer is modeled as an effective resistor and capacitor in parallel, which represent the effective impedance of the current consumer in the power supply time scale.

Those calculations are based on finding the energy stored by the current consumer (*i.e.* effective capacitance) and the power dissipated by the current consumer (*i.e.* effective resistance). The model is based on energy and charge conservation while averaging the current consumer behavior over the clock time period.

The methodology is to find the effective impedance for a maximal switching rate of the current consumer, and then find the actual effective impedance of the current consumer as a fraction of the maximal switching rate. A diagram of the current consumer modeling process is shown in Figure 2. The figure shows a transistor-level microcircuit, which is converted into a linearized equivalent circuit with ideal switches. In the traditional modeling approach, the supply current waveform is calculated from the detailed circuit, and is assigned to an ideal current source. In the proposed new approach, the circuit is represented by a parallel connection of an effective resistance and an effective capacitance, as shown at the bottom right side of the figure.

B. Basic Microcircuit Model

The basic general microcircuit is a CMOS logic gate, which is composed of a pull up path and a pull down path, and therefore can be modeled by an equivalent inverter. The pull up and pull down can be represented by linearized resistances and capacitances (the input capacitances of the next logic stage). Pull up resistance and capacitance are R_1 and C_1 respectively, and pull down resistance and capacitance are R_2 and C_2 respectively [9].

Each resistor is connected in series with an ideal switch. Therefore the resistance of each microcircuit can be characterized as:

$$\frac{1}{R_i(t)} = \begin{cases} \frac{1}{R_i} & Transistor\ i\ is\ On \\ 0 & Transistor\ i\ is\ Off \end{cases} \quad (1)$$

While i is the relevant index (1 or 2 for pull up and pull down respectively) and $R_i(C_1+C_2)$ is the equivalent time constant. This basic microcircuit is shown in Figure 3 (a).

C. Basic Switching Model

In order to develop the model and to calculate the microcircuit effective impedance, first there is a need to calculate the microcircuit effective impedance while fully toggling, *i.e.* while the microcircuit is switching at its maximum frequency rate.

While toggling, one ideal switch is opened and the other is closed. Assume a symmetric infinite toggling, with time period of T, *i.e.* every $T/2$ a toggling occurs. T is in the integrated circuit clock time scale; probably $T/2$ equals the clock time period. T is not necessarily equal for all of the microcircuits and can vary from microcircuit to microcircuit.

Without loss of generality, assume that pull up is ON during the first half of the cycle. This toggling form is shown in Figure 3 (b).

Define the voltage on R_1 and R_2 at time t as $V_1(t)$ and $V_2(t)$ respectively.

In the clock time scale, the supply voltage is constant with the value V_{CC} (changes in the supply voltage occur in the power supply time scale). Therefore The initial conditions ($t=0$) are:

$$V_1(t=0) = V_1(0),\ V_2(t=0) = V_{CC} - V_1(0) \quad (2)$$

In the first half of the toggling ($0<t<T/2$) the voltages are:

$$V_1(t) = V_1(0)\exp\left[-\frac{t}{R_1(C_1+C_2)}\right] \quad (3)$$

$$V_2(t) = V_{cc} - V_1(0)\exp\left[-\frac{t}{R_1(C_1+C_2)}\right]$$

Since the current being consumed from the power supply in the first half of the toggling cycle is the current that flows through C_2:

$$I(t) = C_2\frac{dV_2(t)}{dt} \Rightarrow I(t) = V_1(0)\cdot\frac{C_2}{R_1(C_1+C_2)}\cdot\exp\left[-\frac{t}{R_1(C_1+C_2)}\right] \quad (4)$$

From (3) the voltages in the end of first half of toggling ($t=T/2$) are:

$$\begin{pmatrix} V_1(T/2) \\ V_2(T/2) \end{pmatrix} = \begin{pmatrix} E_1 & 0 \\ 1-E_1 & 1 \end{pmatrix}\begin{pmatrix} V_1(0) \\ V_2(0) \end{pmatrix} \quad (5)$$

Where $E_1 \equiv \exp\left[-\frac{T}{2R_1(C_1+C_2)}\right]$.

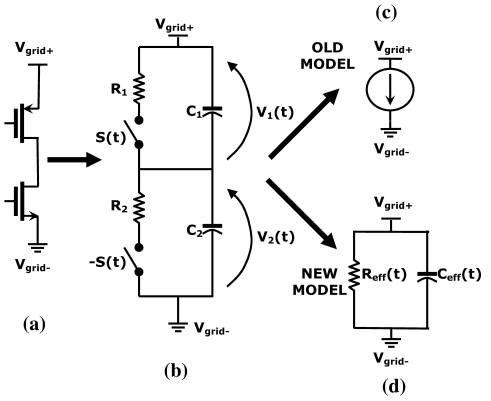


Figure 2. The modeling process of a current consumer. (a) The basic current consumer is a CMOS logic gate, (b) The basic microcircuit model is considering the pull up path and the pull down path represented by a resistor and a capacitor. (c) The conventional model is using an ideal current source to model the current consumer. (d) The roposed model is using effective resistance in parallel to an effective capcitance.

Finding the solution for $V_1(t)$ and $V_2(t)$ for the second half of toggling ($T/2<t<T$) leads to:

$$V_1(t) = V_1(\frac{T}{2}) + V_2(\frac{T}{2})\left\{1-\exp\left[-\frac{t-T/2}{R_2(C_1+C_2)}\right]\right\} \quad (6)$$

$$V_2(t) = V_2(\frac{T}{2})\exp\left[-\frac{t-T/2}{R_2(C_1+C_2)}\right]$$

Since the current being consumed from the power supply in the second half of the toggling cycle is the current that flows through C_1:

$$I(t) = C_1\frac{dV_1(t)}{dt} \Rightarrow I(t) = V_2(\frac{T}{2})\frac{C_1}{R_2(C_1+C_2)}\exp\left[-\frac{t-T/2}{R_2(C_1+C_2)}\right] \quad (7)$$

Combining (5) and (6) leads to:

$$\begin{pmatrix}V_1(T)\\V_2(T)\end{pmatrix} = M\begin{pmatrix}V_1(0)\\V_2(0)\end{pmatrix} \quad (8)$$

Where $E_2 \equiv \exp\left[-\frac{T}{2R_2(C_1+C_2)}\right]$, $M \equiv \begin{pmatrix}E_1+(1-E_1)(1-E_2) & 1-E_2\\ E_2(1-E_1) & E_2\end{pmatrix}$.

D. Steady State Assumption

Since the microcircuit is continuously toggling, it must stabilize in a periodic steady state, *i.e.* the behavior of the microcircuit in every toggling cycle is same as the other cycles. This leads to the boundary conditions that the voltages in the beginning and ending of each cycle are equal:

$$\begin{pmatrix}V_1(T)\\V_2(T)\end{pmatrix} = \begin{pmatrix}1 & 0\\0 & 1\end{pmatrix}\begin{pmatrix}V_1(0)\\V_2(0)\end{pmatrix} \quad (9)$$

From (8) and (9):

$$(M-I)\begin{pmatrix}V_1(0)\\V_2(0)\end{pmatrix} = 0 \quad (10)$$

Since the determinant of M-I is 0, M-I is singular and therefore (10) has non trivial solution.

E. Delivered Charge

The charge delivered to the microcircuit in every toggling cycle is calculated based on the definition of charge as the integral of the current over time, using (4), (6), (7) and (8):

$$Q = \int_0^T dtI(t) = Q_1(0)[1-E_1]\cdot\frac{C_2}{C_1} + Q_2(0)\cdot\frac{1-E_2}{E_2}\cdot\frac{C_1}{C_2} \quad (11)$$

Where $Q_1(0)=C_1V_1(0)$ and $Q_2(0)=C_2V_2(0)$.
From (8) and (10) the ratio between the initial voltages is:

$$V_2(0) = E_2\cdot\frac{1-E_1}{1-E_2}\cdot V_1(0) \quad (12)$$

Inserting (12) to (11)**Error! Reference source not found.** leads to:

$$Q = (C_1+C_2)\cdot V_1(0)\cdot(1-E_1) \quad (13)$$

F. Energy Dissipation

By definition, the energy being dissipated by the microcircuit every toggling cycle is the energy being dissipated by R_1 and R_2 in the first and second halves of the toggling cycle respectively:

$$W_D = \frac{1}{R_1}\int_0^{T/2} V_1^2(t)dt + \frac{1}{R_2}\int_{T/2}^{T} V_2^2(t)dt \quad (14)$$

From (3), (6), (12) and (14) the energy being dissipated by the microcircuit every toggling cycle is:

$$W_D = (C_1+C_2)V_1(0)^2\frac{1-E_1}{1-E_2}[1-E_1E_2] \quad (15)$$

G. Effective Impedance for Maximum Switching Rate

From (2) and (12) the initial voltages condition can be calculated in term of V_{CC}:

$$V_1(0) = \frac{1-E_2}{1-E_1E_2}\cdot V_{CC}, \quad V_2(0) = E_2\cdot\frac{1-E_1}{1-E_1E_2}\cdot V_{CC} \quad (16)$$

Inserting (16) to (13) leads to:

$$Q = (C_1+C_2)\cdot\frac{(1-E_1)(1-E_2)}{1-E_1E_2}V_{CC} \quad (17)$$

Inserting (16) to (15) leads to:

$$W_D = (C_1+C_2)\frac{(1-E_1)(1-E_2)}{1-E_1E_2}V_{CC}^2 \quad (18)$$

The calculation above was done in the clock time scale (picoseconds or nanoseconds) and presents the exact charge delivered and dissipated energy.
The charge delivered can be modeled as the charge being stored by a capacitor and the dissipated energy can be modeled as the total power dissipation of a resistor. The impedance value of the resistor and capacitor is constant in the clock time scale and its value can be calculated from the averaging of one toggling cycle T. The impedance value can be changed slowly in the power supply time scale.
Therefore, the effective impedance for maximum switching rate is a capacitor in parallel to a resistor. The effective capacitance for maximum switching rate is by definition the charge divided in the supply voltage, using (17) leads to:

$$C_0 = \frac{Q}{V_{CC}} = (C_1+C_2)\frac{(1-E_1)(1-E_2)}{1-E_1E_2} \quad (19)$$

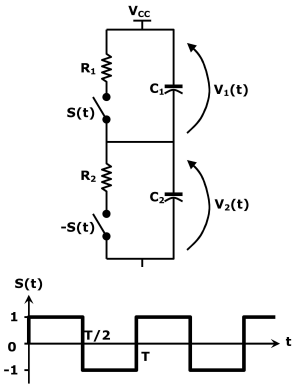
The effective resistance for maximum switching is calculated from the energy dissipation, using (18):

$$R_0 = \frac{V_{CC}^2}{W_D}\cdot T = \frac{1-E_1E_2}{(C_1+C_2)(1-E_1)(1-E_2)}\cdot T = \frac{T}{C_0} \quad (20)$$

While the result in (20) is simple, it is not obvious. It is reasonable to assume that the product of R_0 and C_0 is a constant; however, this constant is not necessarily T. From (20) one can determine the model parameters only from two parameters out of the 3 (T, R_0 and C_0). Furthermore, since the value of E_1 and E_2 is in most cases small, the effective capacitance is similar to the sum of C_1 *and* C_2, so knowing T, C_1 *and* C_2 is enough for most cases.

H. Macro Circuit

Subject to the assumptions above, this microcircuit model exactly represents the energy consumption of the original gate circuit, and this main feature is naturally expandable to hundreds of thousands or millions of microcircuits, which acts in parallel. This is the essence of the model.



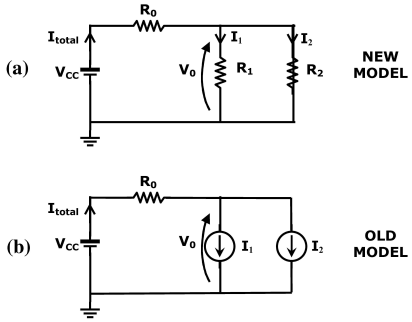


Figure 4. Two macro circuits connected to a power grid with resistance of R_0 (a) The macro circuits are modeled in the proposed model with effective resistance R_1 and R_2, the effective capacitance is not mentioned since it is disconnected in DC. (b) The macro circuits are modeled as ideal current sources I_1 and I_2.

The extension of the model can be done for a large number of microcircuits with similar/identical switching characterization (the same clock, close one to each other, connected to the same node in the grid).

Assume there are N microcircuits connected to the same node in the grid (all of them are connected in parallel), with an effective resistance and effective capacitance for maximum switching rate $R_{0,i}$, $C_{0,i}$ for the i microcircuit ($i=1,\ldots,N$). This situation equivalent to a single macro circuit connected to the node with the effective impedance for maximum switching rate:

$$R_0 = R_{0,1} \parallel R_{0,2} \parallel \ldots \parallel R_{0,N} \qquad (21)$$
$$C_0 = C_{0,1} + C_{0,2} + \ldots + C_{0,N}$$

I. Activity Function and Effective Impedance

The actual toggling rate of different macro circuits is typically not the maximum rate, but a portion of it. Since the effective impedance indicates the total energy dissipation and stored charge of the macro circuit, the activity factor of the macro circuit, which indicates its switching rate as a fraction of the maximum switching rate, can be used [8], [11].

In the clock time scale the switching rate in steady state is constant, *i.e.* the time constant is constant:

$$\mathrm{R}_{eff}\, C_{eff} = const \qquad (22)$$

In the power supply time scale the fraction from maximum switching rate can change and therefore it is more appropriate to describe that fraction as activity function, rather than activity factor.

In order to model the actual behavior of the macro circuits, the effective capacitance for maximum switching rate is multiplied by the activity function of the macro circuit and the effective resistance for maximum switching rate is divided by the activity function of the macro circuit. Therefore the effective impedance is:

$$C_{eff} = C_0 \cdot \alpha(t), \quad R_{eff} = R_0 \cdot \frac{1}{\alpha(t)} \qquad (23)$$

Where C_0 and R_0 are the effective capacitance and resistance for maximum switching rate, respectively, calculated in (21) and $\alpha(t)$ is the activity function of the macro circuit (t is the time in the power supply time scale).

Equation (23) shows that (22) is being observed. When the macro circuit is at maximum switching rate mode, $\alpha(t)$ equals 1 and therefore the effective impedance equals the effective impedance for maximum switching rate from (21). When the macro circuit is off (no switching at all), $\alpha(t)$ equals 0, no power being dissipated and no energy being accumulated, in this case the effective capacitance is zero (can not store any energy) and the effective resistance is infinity (can not dissipate any power). The dynamic behavior of the power grid and can be analyzed by characterization of the dynamic behavior of the switching function $\alpha(t)$ at the time scale of the power supply.

III. Feedback between the Power Grid and Current Consumer

Voltage drops in the grid are caused by currents flowing through the grid. The decrease in the voltage supplied to logic gates lowers the current drawn from the current supply and therefore there is negative feedback between the power supply current and the power supply noise.

The ideal current source model ignores this interaction, and therefore the voltage drop predicted by this model is unrealistically high.

In the proposed model, since only passive elements are used, when the supply voltage is lowered, the current is reduced due to Ohm's law.

A toy example demonstration is shown in Figure 4. Assume that two macro circuits are connected to a power grid with a resistance R_0 and a negligible inductance. In the initial conditions in every macro circuit the currents flowing are I_1 and I_2 and effective resistances are R_1 and R_2, respectively. In order to get compatibility between the two models the current flown in each current consumer satisfies Ohm's law. The initial voltage V_0 is equal in both models and it is a simple voltage divider:

$$V_0 = V_{CC} - (I_1 + I_2) R_0 = \frac{R_1 \parallel R_2}{R_0 + R_1 \parallel R_2} \cdot V_{CC} \qquad (24)$$

Now, assume a change occurs only in one macro circuit, its effective resistance is lowered (higher activity function) and therefore it consumes more current. The parameters of the second macro circuits are unchanged.

In the new proposed model, the change in the circuit can be described by the change in the first macro circuit effective resistance:

$$\tilde{R}_1 = R_1 - \Delta R \qquad (25)$$

The voltage V_0 is a simple voltage divider with the new values of the resistors:

$$V_0 = \frac{(R_1 - \Delta R) \parallel R_2}{R_0 + (R_1 - \Delta R) \parallel R_2} \cdot V_{CC} \qquad (26)$$

In the ideal current source model, the current I_2 is unchanged and the value of the new current I_1 is:

$$I_1 = \frac{V_{CC}}{R_0 + R_1 \parallel R_2} \cdot \frac{R_1 \parallel R_2}{R_1 - \Delta R} \qquad (27)$$

And the voltage V_0 in the ideal current source model is:

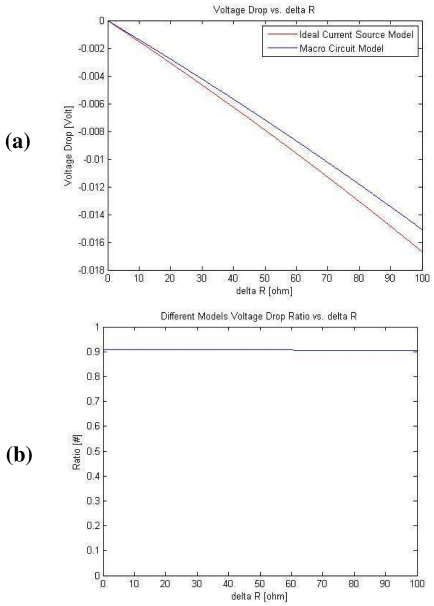


Figure 5. The results for the interaction example. In this example V_{CC}=3.3V, R_0=50 ohm, R_1=1kohm, R_2=1kohm.(a) The calculated voltage drop for the old and new models for various changes in the effective resistance of the first macro circuit (decrease in R_1). (b) The ratio between the voltage drop in the new model and the old model. It is almost constant with an average ratio of 90.6%.

$$V_0 = V_{CC}\left[1 - \frac{R_0}{R_0 + R_1 \| R_2} \cdot \frac{R_1}{R_1 - \Delta R} \cdot \frac{R_1 - \Delta R + R_2}{R_1 + R_2}\right] \qquad (28)$$

The voltage drop is the difference between the value of the initial voltage in (24) and the value of the voltage after the changes in (26) and (28), respectively.

In Figure 5 and Figure 6 the results for this case are shown. The voltage drop of the proposed model is lower than the voltage drop in the old model. The negative feedback phenomenon is rising in power grids with higher impedance (high value of R_0), as the resistance of R_0 is rising, the difference in the voltage drop between the model increases (up to 50% in our example in Figure 6).

IV. Discussion

In the microcircuit model we did not take into account decoupling capacitors and those capacitors needs to be taken as part of the effective capacitance of the microcircuit.

The activity function of a macro circuit is a statistical function. In order to get realistic effective impedance, the activity function needs to be characterized, based on real integrated circuits and to be determined as a statistical function. Furthermore, it is reasonable to believe that it is possible to determine an equivalent meta-macro circuit with a meta-activity function that determines the behavior of the whole macro circuits together.

V. Conclusion

A new model for current consumers in power grids and a new methodology for automatic design of power grids are presented in this paper. The current consumer model is based on energy conservation. In the current consumer model, microcircuits are determined as the effective impedance of the current consumer, while toggles at maximum switching rate and macro circuits are determined as a cluster of microcircuits, while it is toggling in its actual toggling rate.

An example of how the proposed model takes into account

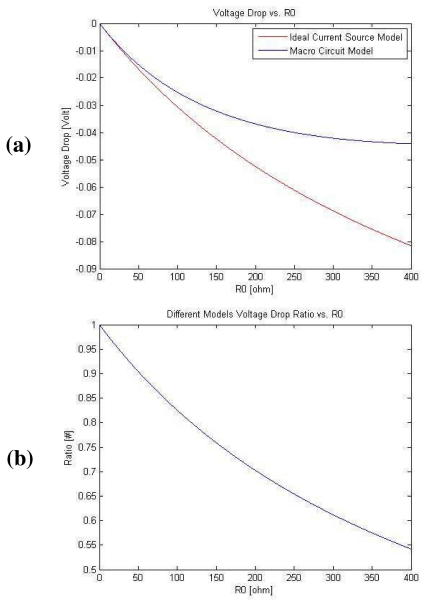


Figure 6. The results for the interaction example. In this example V_{CC}=3.3V, delta_R=100 ohm, R_1=1kohm, R_2=1kohm.(a) The calculated voltage drop for the old and new models for various changes in the resistance of the grid (changes in R_0). (b) The ratio between the voltage drop in the new model and the old model. The negative feedback phenomenon is rising as the grid becomes less optimal (higher R_0).

interactions between the power grid and the current consumer has been presented. The voltage drop in the proposed model is lower than the voltage drop in the old model and the differences increase as the power grid resistance is rising.

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