Power and Area Efficient Network-on-Chip Architectures

SRC TASK 1204.001

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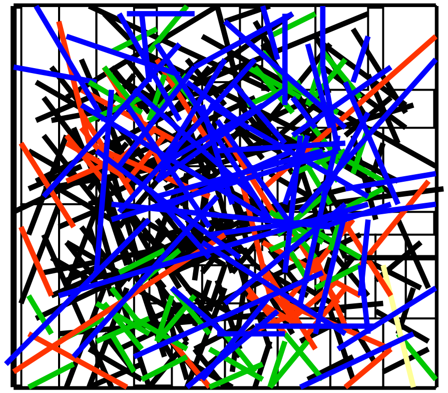
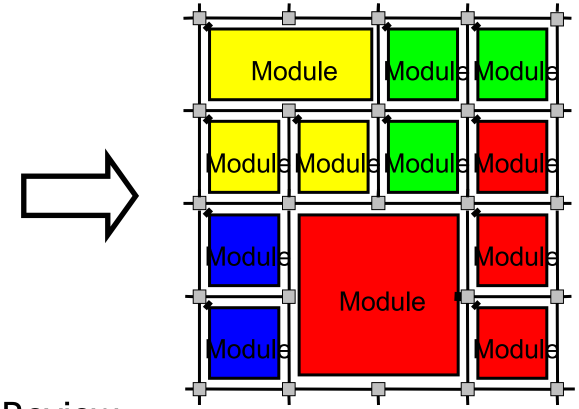
Research Objective

Power and Area Efficient Network on Chip (NoC):

- Network layer architecture
  - ✓switching techniques
  - ✓routing
  - ✓congestion control
  - ✓topology
- Fast on-chip communication links
- Circuit design for NoC components





The Team

- **Faculty:**
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- **SRC monitor:** David C. Yeh

- **Funding (in part):** SRC/Freescale, Intel, Ceva-DSP

Industrial Cooperation

- Presentations and discussions with
  - **Freescale**
  - **Intel**
  - Zoran
  - Ceva-DSP
  - Mellanox
  - Connexant
  - EZ-Chip

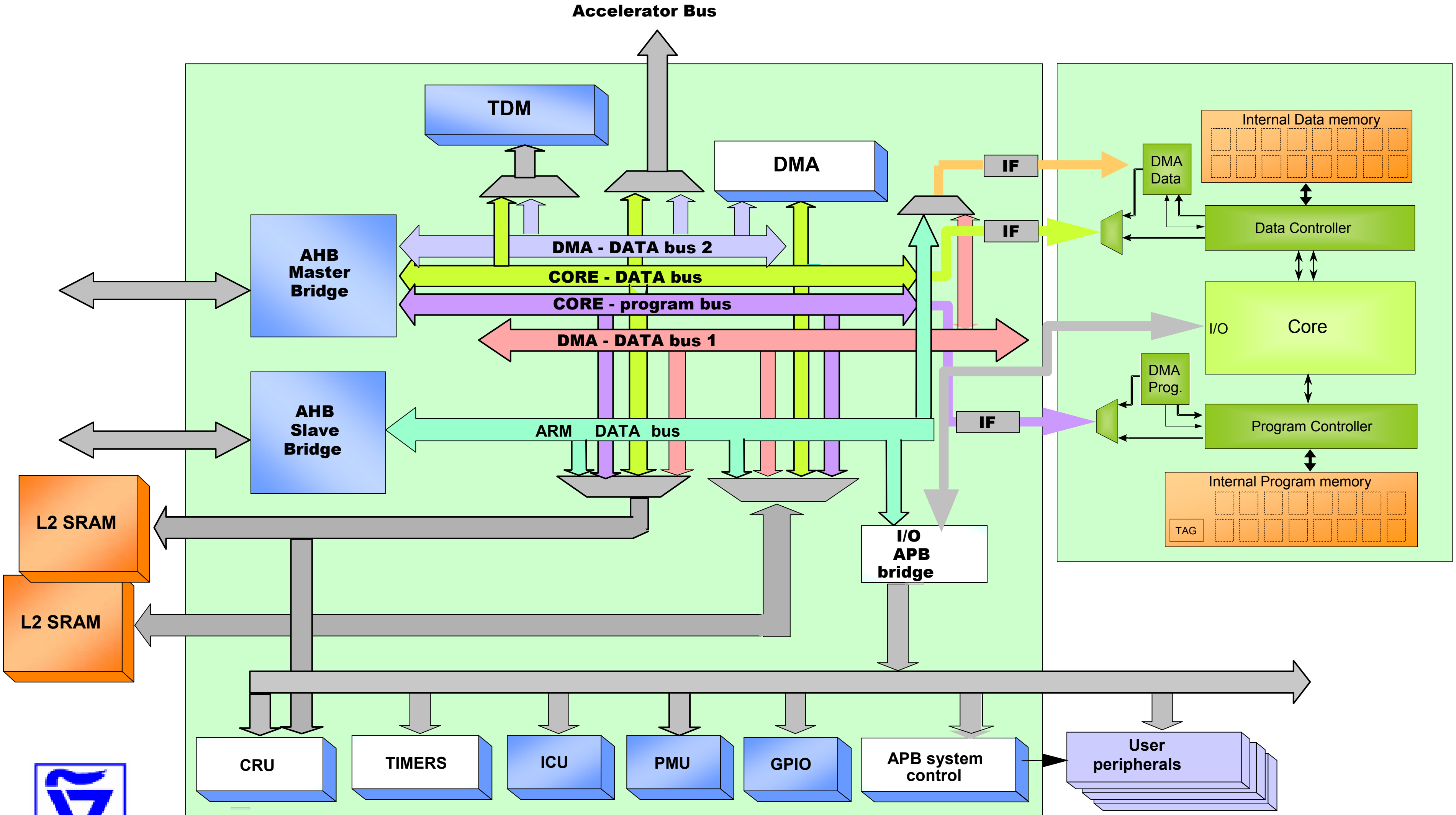
Publications

- E. Bolotin, I. Cidon, R. Ginosar, A. Kolodny, "QNoC: QoS architecture and design process for network on chip," Special issue on Networks on Chip, The Journal of Systems Architecture, 50(2-3):105-128, February 2004.
- E. Bolotin, I. Cidon, R. Ginosar, A. Kolodny, "Cost considerations in network on chip," Integration—the VLSI Journal, 38(1):19-42, Oct. 2004.
- A. Morgenshtein, E. Bolotin, I. Cidon, A. Kolodny, R. Ginosar, "Micro-Modem – Reliability Solution for NoC Communications," Proc. ICECS 2004.
- E. Bolotin, A. Morgenshtein, I. Cidon, R. Ginosar and A. Kolodny, "Automatic Hardware-Efficient SoC Integration by QoS Network on Chip," Proc. ICECS 2004.
- A. morgenshtein, "Comparative Analysis of Serial vs Parallel Links in Networks on Chip," Proc. SoC 2004.
- R. Dobkin, V. Vishnyakov, E. Friedman and R.Ginosar, "An Asynchronous Router for Multiple Service Levels Networks on Chip," Proc. ASYNC 2005.
- R. Dobkin, I.Cidon, R.Ginosar, A.Kolodny and A.Morgenshtein, "Fast Asynchronous Bit-Serial Interconnects for Network-on-Chip," Internal Technical Report, 2004.
- A. Morgenshtein, I.Cidon, A. Kolodny and R. Ginosar, "Low-Leakage Repeaters for NoC Interconnects," Proc. ISCAS 2005.

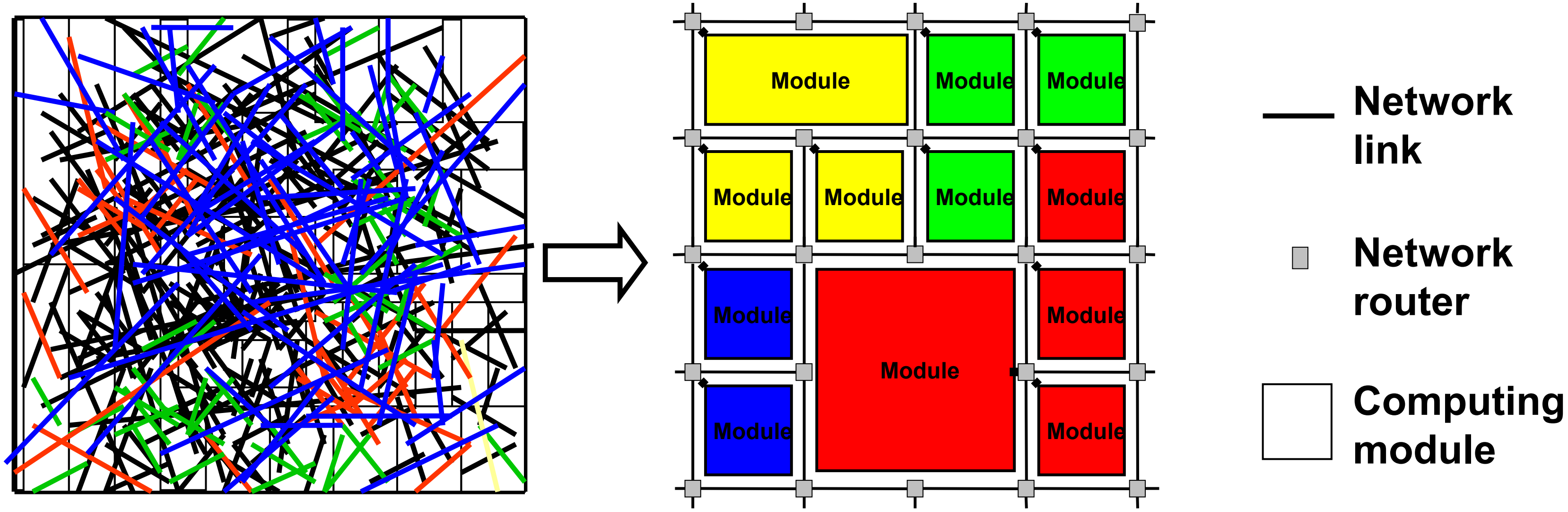
Presentation Outline

- **Research motivation**
  - **Problems**
  - **Advantages of NoC**
  - **Scalability analysis**
  - **Challenges**
- Results of 2004
- Future work

Problems in Evolutionary Approach to SOC



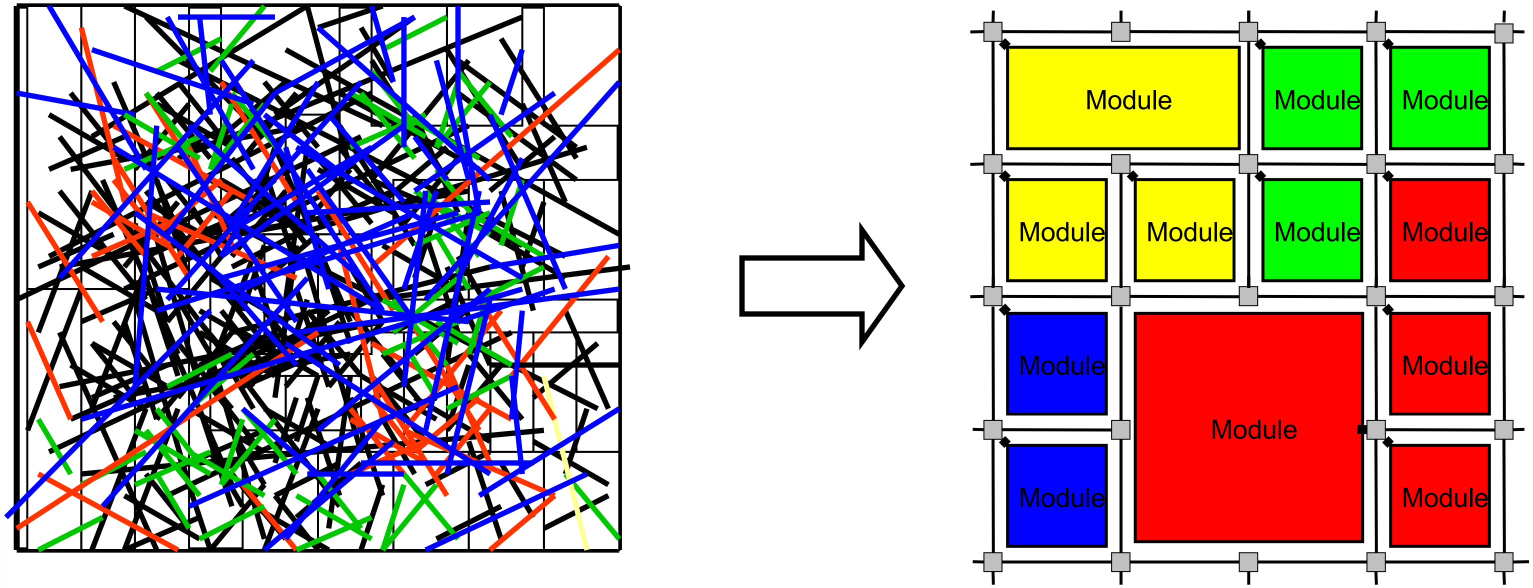
NoC Paradigm Advantages



- Efficient sharing of wires
- Lower cost / lower risk / faster design
- Scalability
- NoC employs statistical multiplexing via packets
- NoC is an infrastructure (e.g. power, clock)
- NoC is customized for each chip

NoC: Why Now?

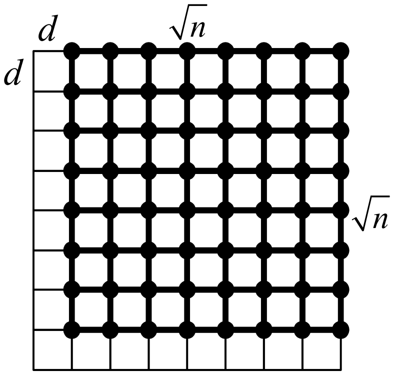
- Global interconnect delay, noise, power
- Full-chip productivity crisis
- Chip Multi-Processors



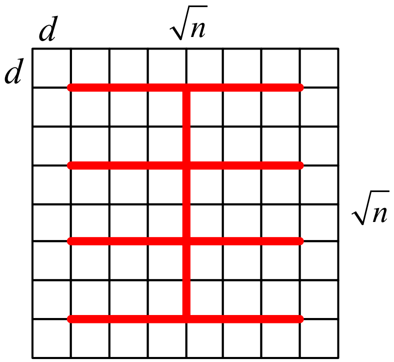
NoC scalability vs. alternatives

For Same Performance, compare the cost of:

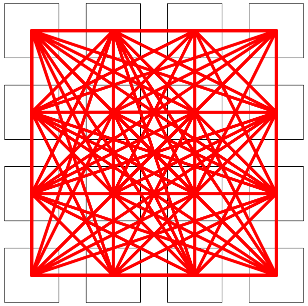
NoC:



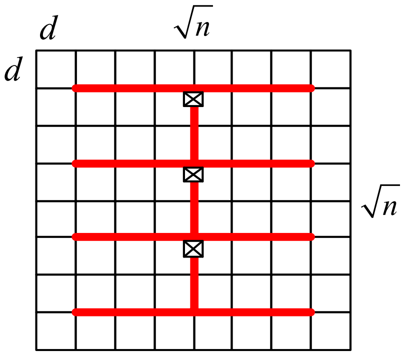
Non-Segmented Bus:



Point-to-Point:

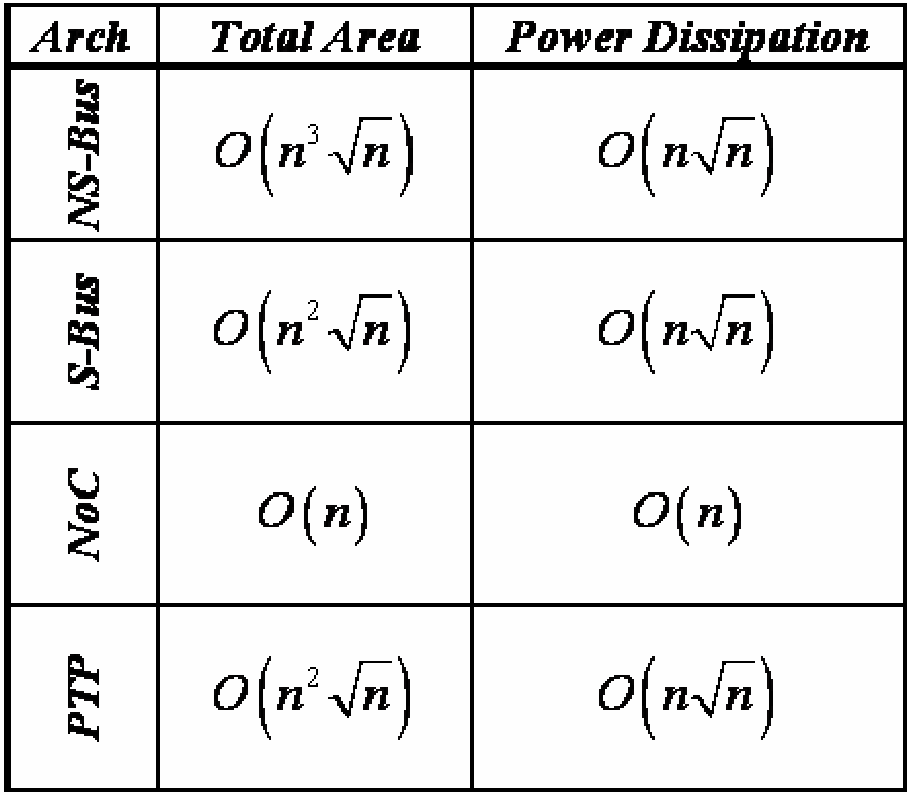


Segmented Bus:



Asymptotic cost scalability

Power and Area required to provide same bandwidth versus number of system modules n



Arch	Total Area	Power Dissipation
NS-Bus	$O\left(n^3\sqrt{n}\right)$	$O\left(n\sqrt{n}\right)$
S-Bus	$O\left(n^2\sqrt{n}\right)$	$O\left(n\sqrt{n}\right)$
NoC	$O\left(n\right)$	$O\left(n\right)$
PTP	$O\left(n^2\sqrt{n}\right)$	$O\left(n\sqrt{n}\right)$

* E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny, "Cost Considerations in Network-on-Chip", INTEGRATION – the VLSI journal, 2004)

NoC Challenges

- Low cost:
  - Area (routers, interfaces and links)
  - Power (dynamic, leakage)
- Flexible standard interface
- Multiple levels of service (QoS)
  - Throughput
  - End-to-end delay
- Low design effort

Presentation Outline

- Research motivation
- **Results of 2004**
  - **QNoC architecture**
  - **Design flow for a QNoC-based system**
  - **Circuit level aspects: links and routers**
- Future work

QNoC: Quality-of-service NoC architecture

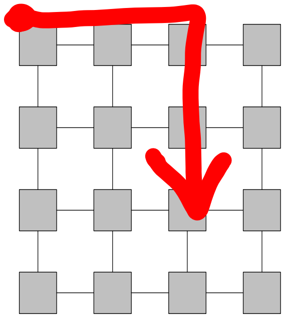
Define Service Levels like:

- *Signaling – interrupts, signals.*
- *Real-Time - audio, video.*
- *Read/Write (RD/WR) – bus semantics*
- *Block-Transfer – DMA semantics*

✓ Different QoS **(delay characteristics)** for each Service Level

* E. Bolotin, I. Cidon, R. Ginosar and A. Kolodny., **"QNoC: QoS architecture and design process for Network on Chip"**, JSA special issue on NoC, 2004.

QNoC topology and routing-path

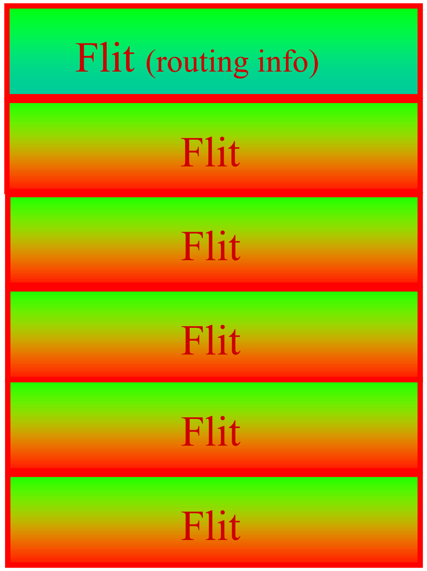


- Mesh topology
  - ✓ Variable capacity links
- Fixed shortest path routing (X-Y)
  - ✓ Simple Router (no tables, simple logic)
  - ✓ No deadlock scenario
  - ✓ No retransmission
  - ✓ No reordering of messages
  - ✓ Power-efficient

Wormhole routing

- For reduced buffering
- Reduced Latency
- Simple router hardware
- Virtual channels enable variable link speeds

Wormhole Packet:



Flit (routing info)

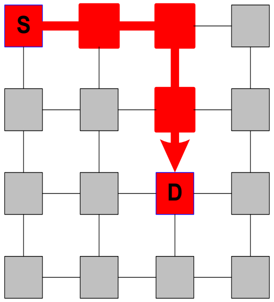
Flit

Flit

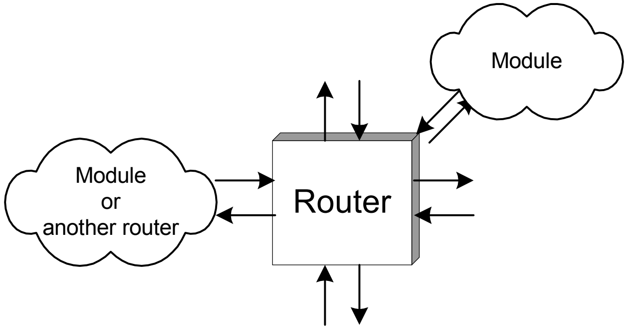
Flit

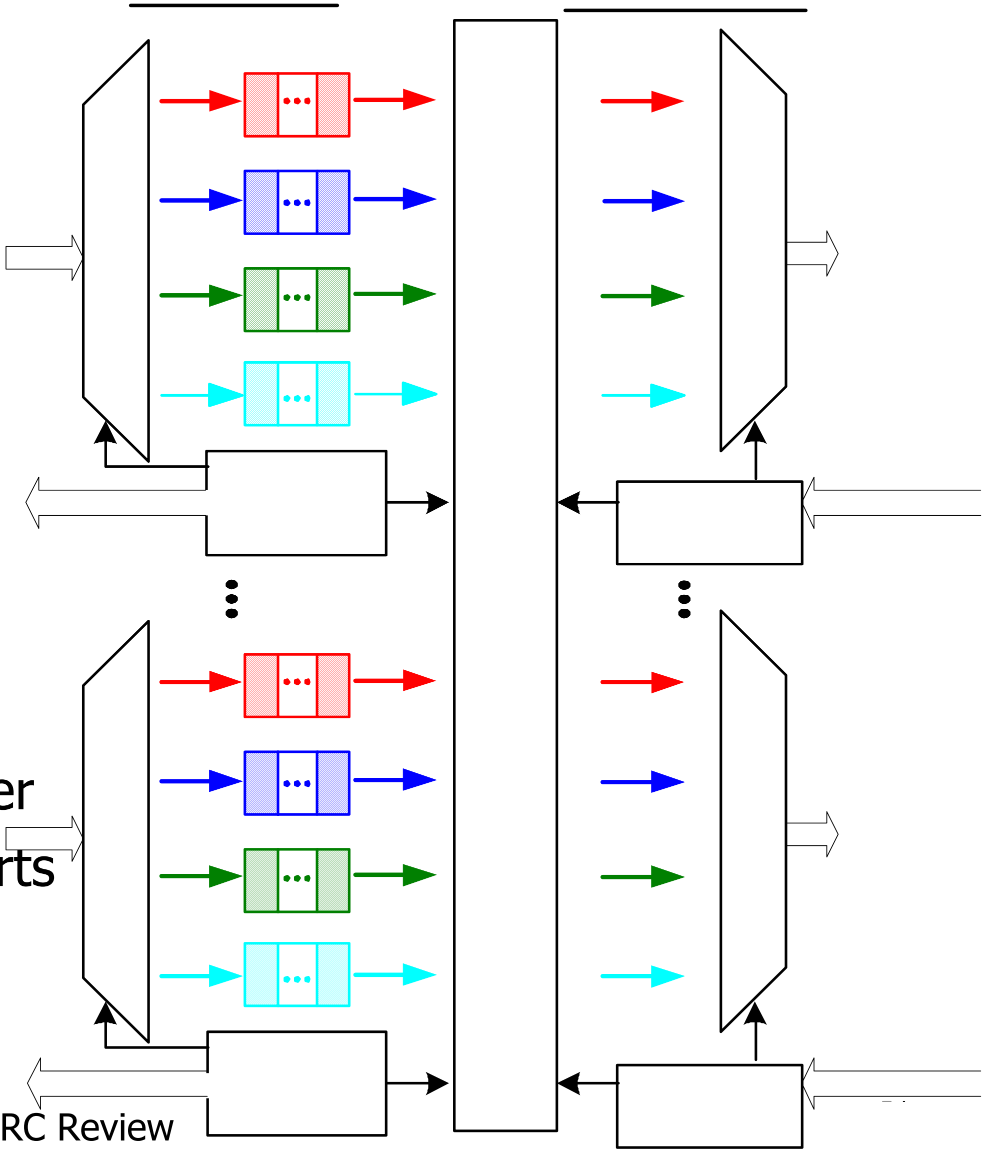
Flit

Flit



Router structure

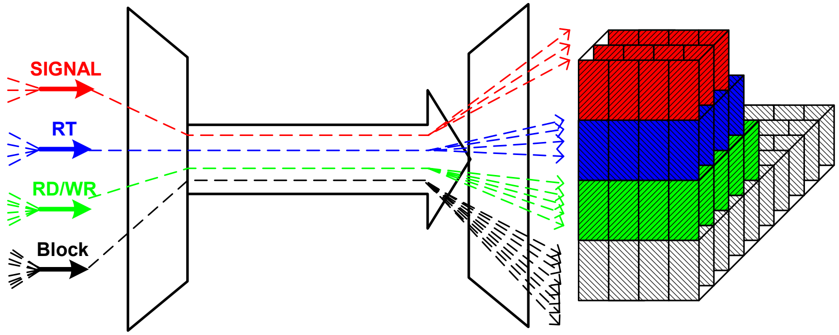




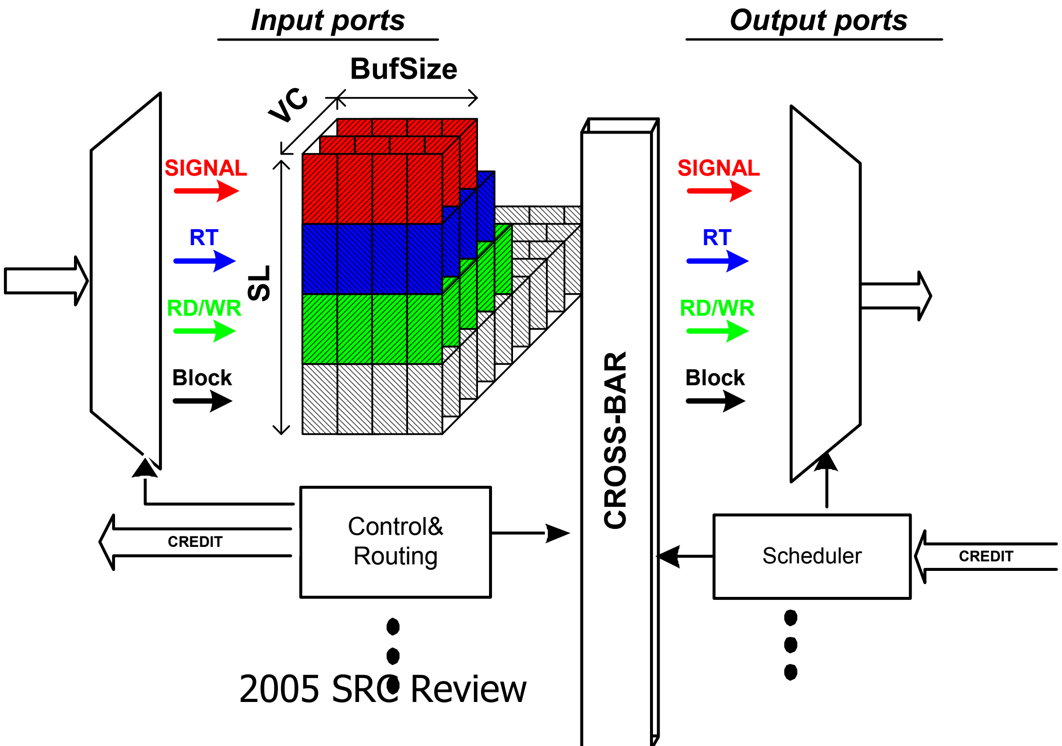
- Flits stored in input ports
- Output port schedules transmission of pending flits according to:
  - Priority (*Service Level*)
  - Buffer space in next router
  - Round-Robin on input ports of same SL
  - Preempt lower priority packets

QNoC router with multiple Virtual Channels

Multiple VCs link:



The QNoC Router:

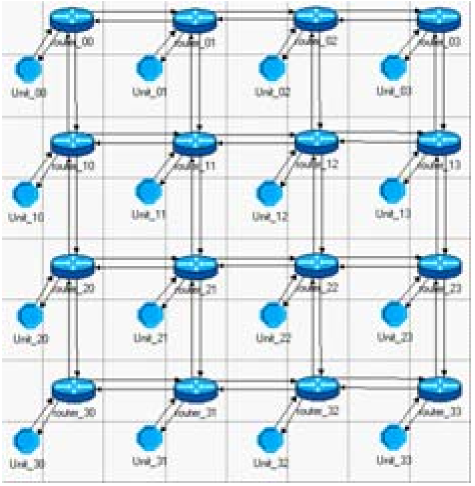


Simulation Model

- OPNET Models for QNoC:
  - Node (Source/Sink)
  - Router
  - Port
  - Link
- Any topology and traffic load
- Statistical traffic generation at source nodes
- Flit level simulations

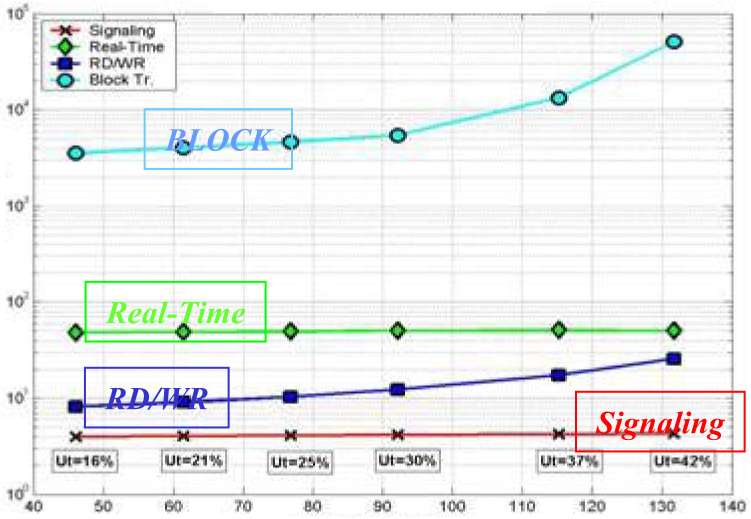
Simulation example

QNoC Example:



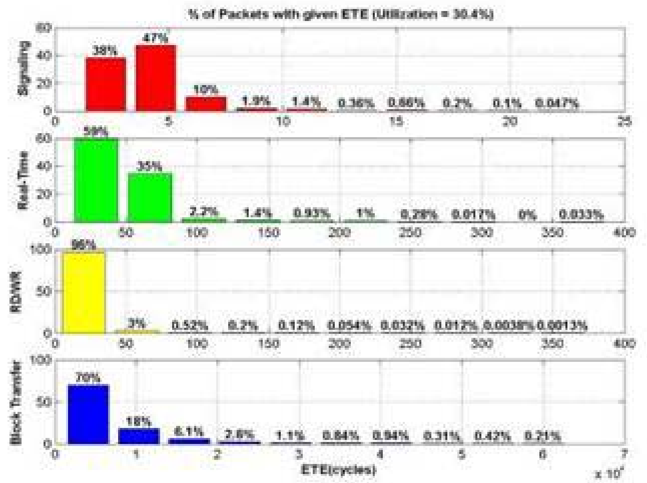
Results Example:

ETE Delay



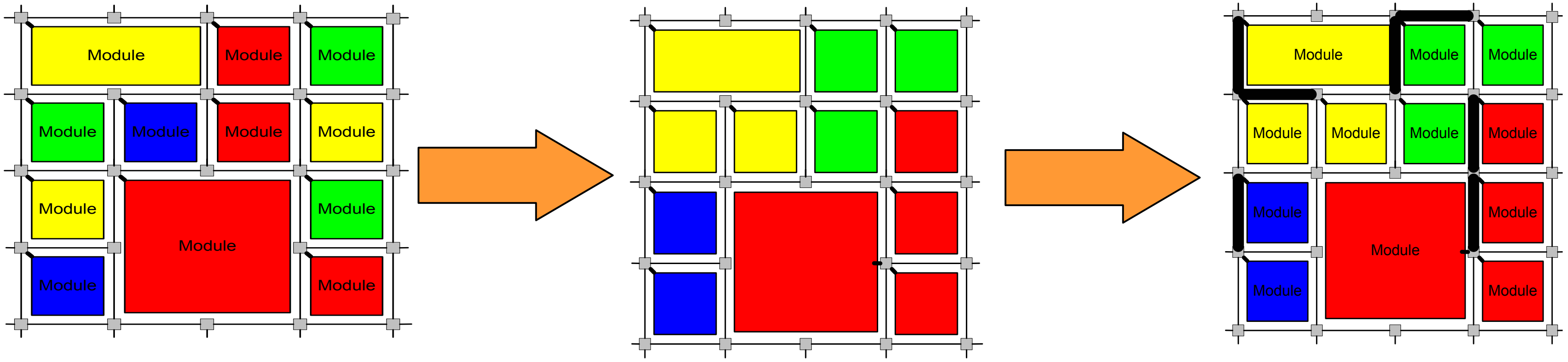
Traffic Load

%Packets



Delay

NoC Customization



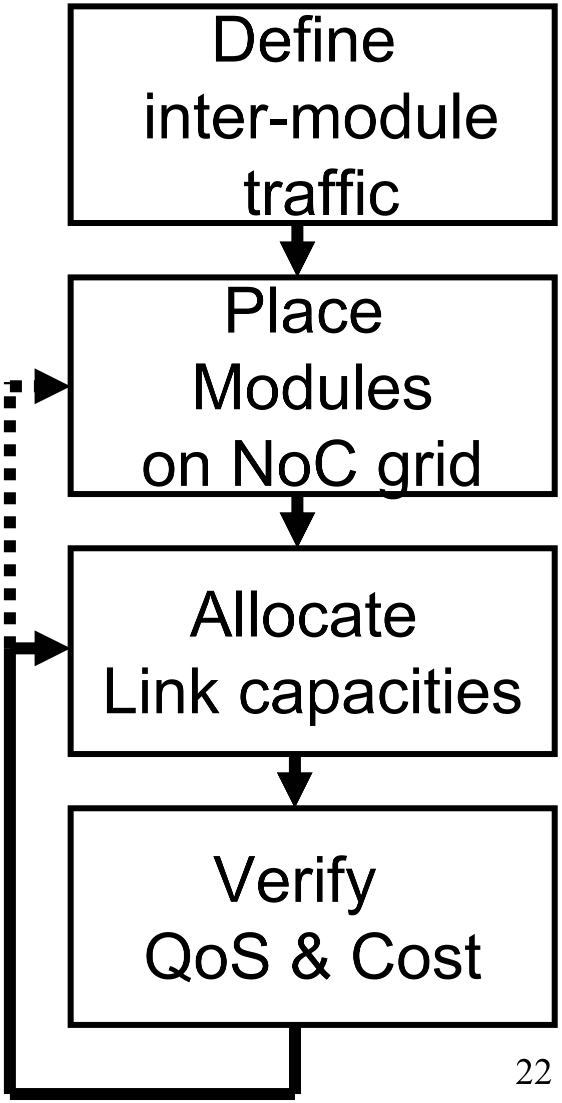
Place
Modules

Trim
routers / ports / links

Adjust link
capacities

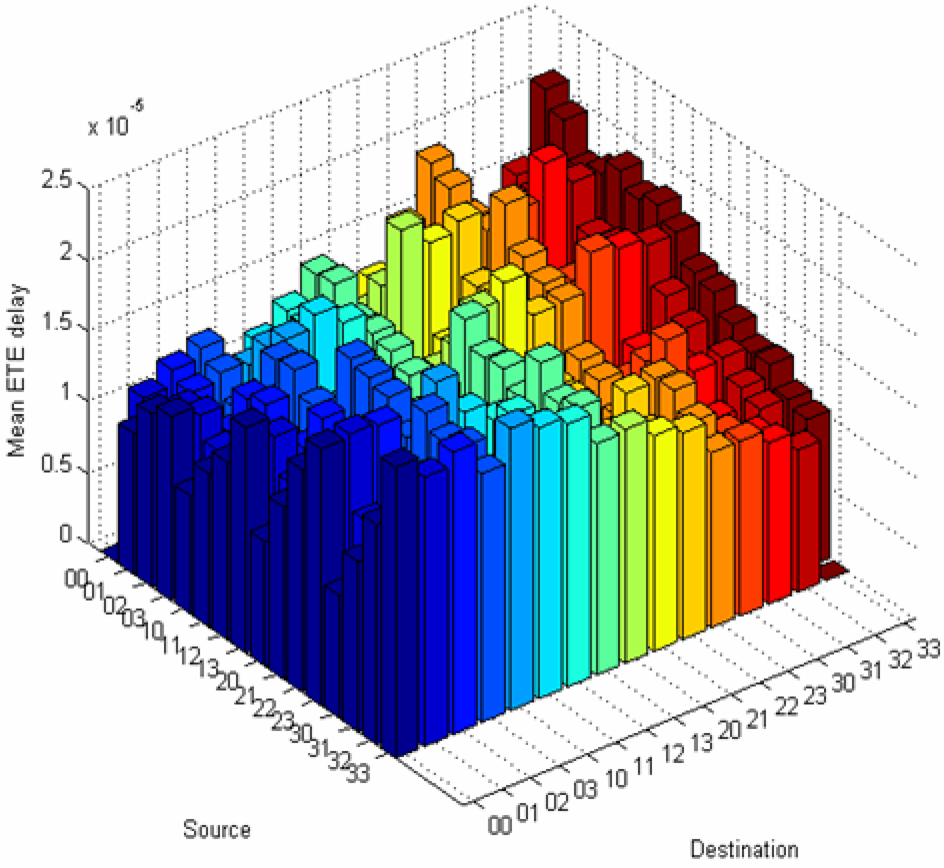
QNoC-based System Design Flow

- Behavioral simulation with “ideal network”
  - Define traffic requirements
- Placement
  - NoC Cost function
- Adjust link capacities
  - Satisfy QoS
  - Use analytical delay estimation
- Verify timing by statistical simulation on full network model



Capacity Allocation Problem

- Classical wormhole networks: uniform link capacity
  - Simple but delay unbalanced!
- Slacks should be minimized
- Optimization problem:



Simulated mean packet delays in a 4-by-4 uniform network

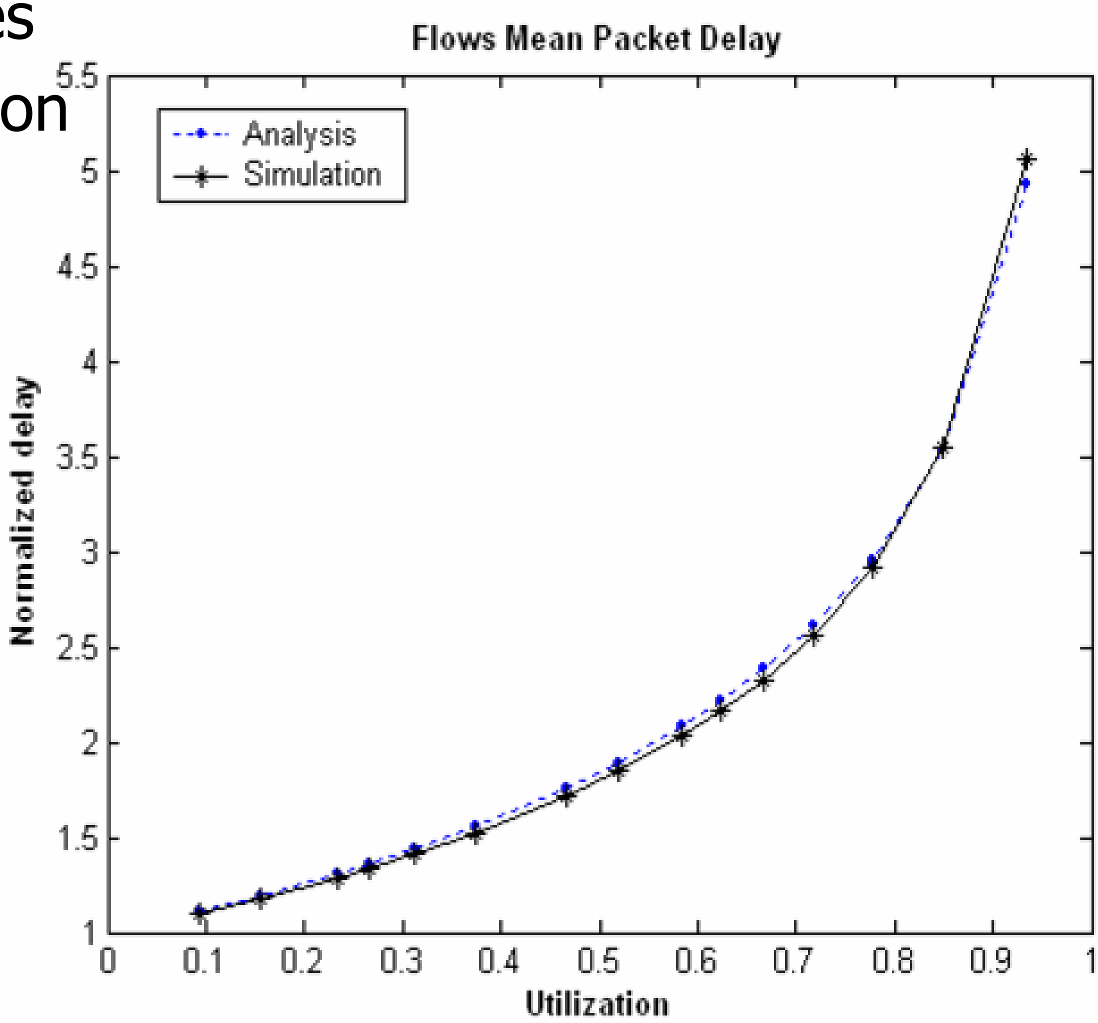
- Given:
  - system topology and routing
  - Each flow's bandwidth (f^i) and delay bound (T^i_{REQ})
- Minimize total link capacity $\left(\sum_{e \in E} C_e\right)$
- Such that:

$$\forall link\ e: \quad \sum_{i | e \in path(i)} f^i < C_e$$

$$\forall flow\ i: \quad T^i \le T^i_{REQ}$$

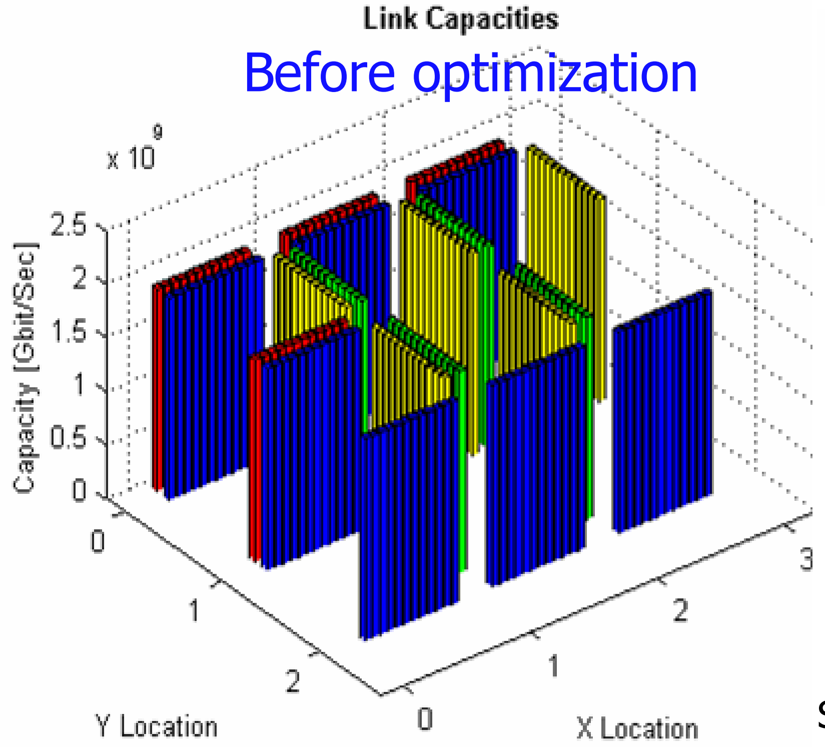
Network Delay Model

- Analysis of mean packet delay in wormhole network
  - Multiple Virtual-Channels
  - Different link capacities
  - Different communication demands
- Iteratively use the analysis to allocate capacities subject to delay requirements



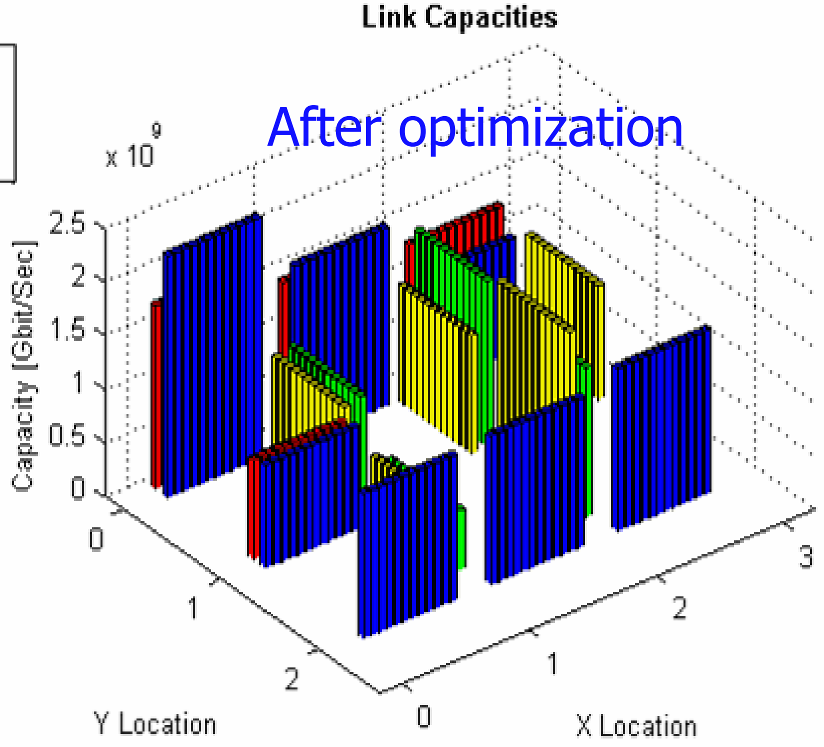
Capacity Allocation Example

- A SoC-like system with specific traffic demands and delay requirements
- “Classic” design: 41.8Gbit/sec
- Using the algorithm: 28.7Gbit/sec
- Total capacity reduced by 30%



Before optimization

🟦 Right
🟥 Left
🟨 Down
🟩 Up



After optimization

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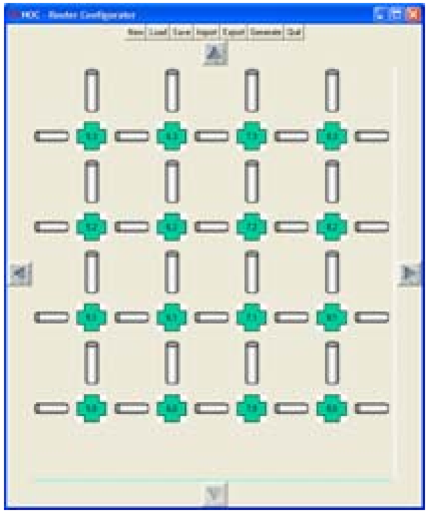
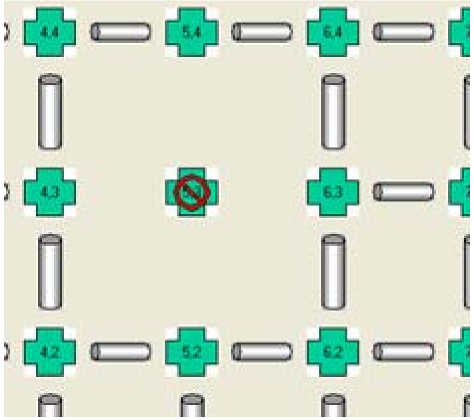
QNoC VHDL Hardware Generation Tool

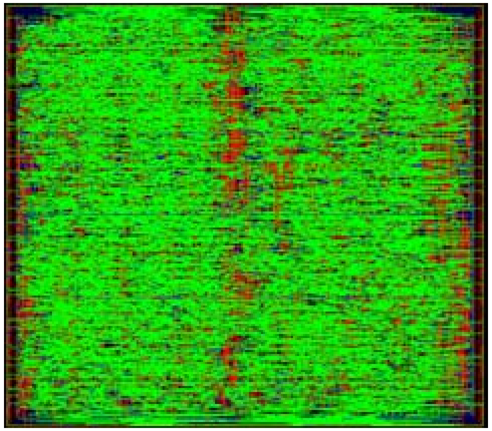
Standard Topology Example:



Custom Topology Example:



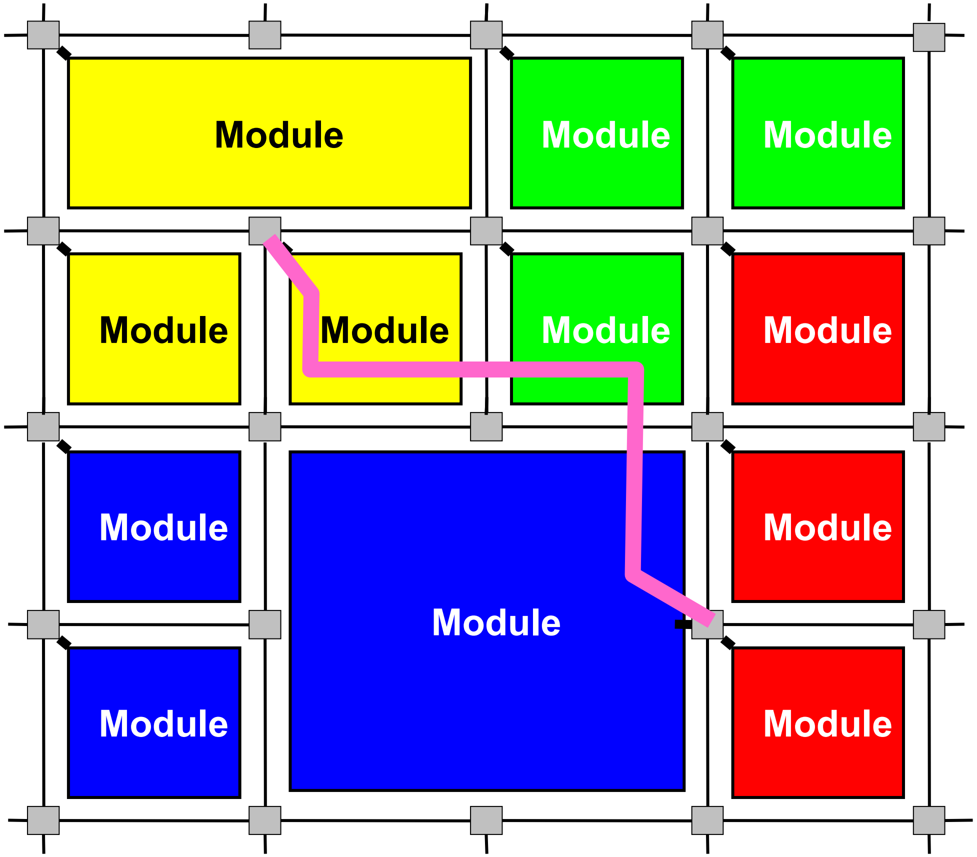
Router Layout:



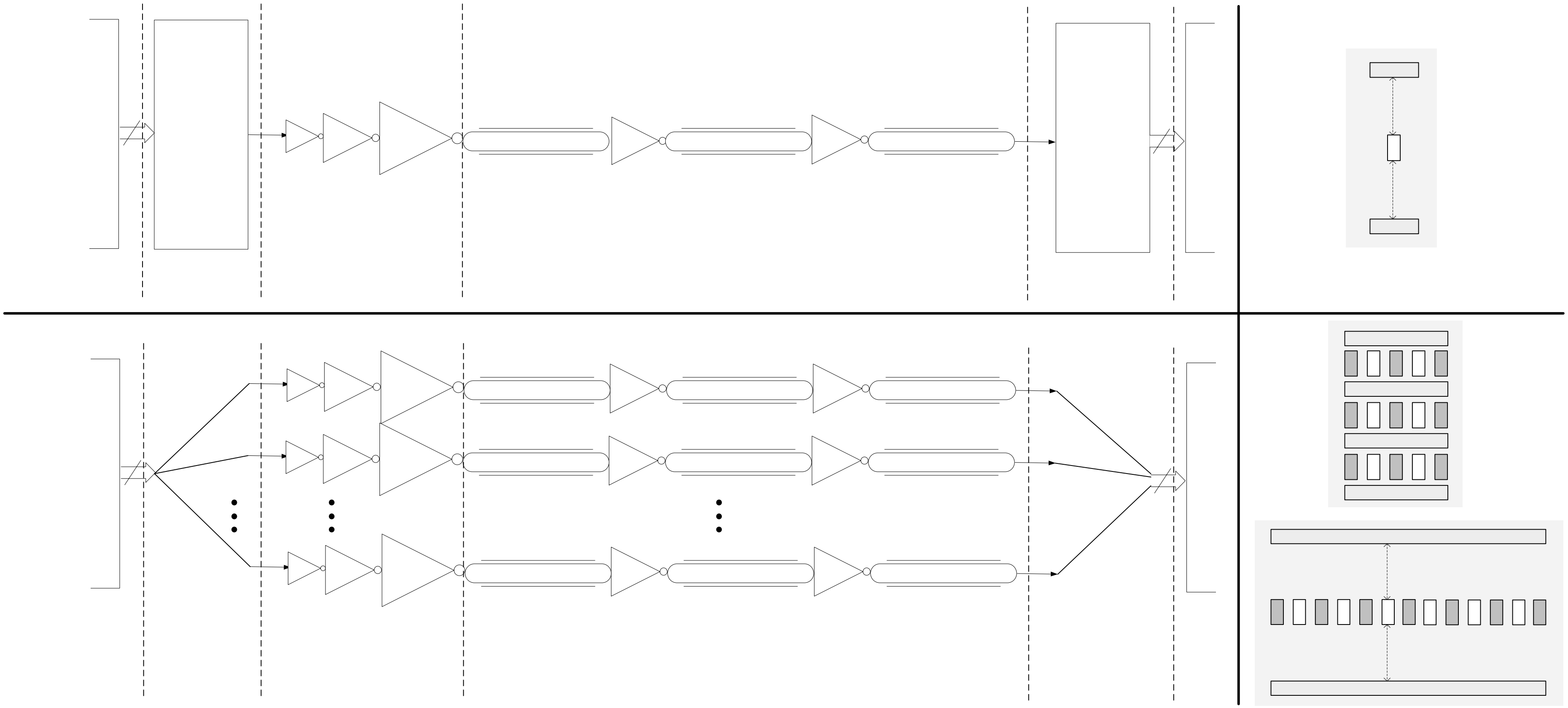
Synthesis results for various routers (Mosis 0,35 um):

Number of ports	Area [μm^2]
2	1,323,955
3	1,720,618
4	2,117,281
5	2,513,964

Long-haul serial links?



Comparing Serial & Parallel Links



* A. Morgenshtein, I. Cidon, A. Kolodny, R. Ginosar, **“Comparative Analysis of Serial and Parallel Links in Networks-on-Chip”**, SoC 2004

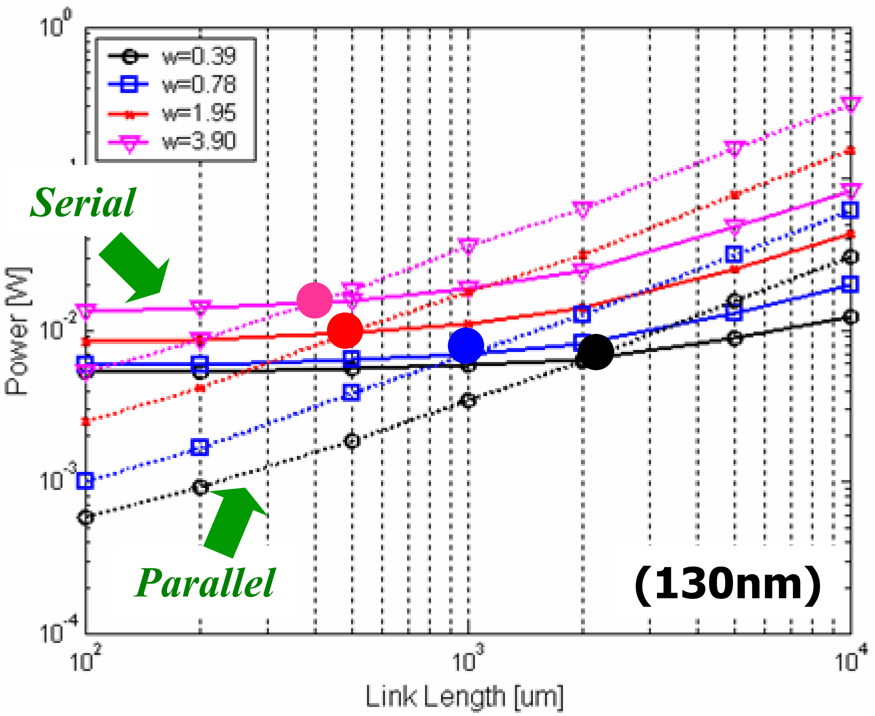
$h_{cas_{ser}}$, $k_{cas_{ser}}$

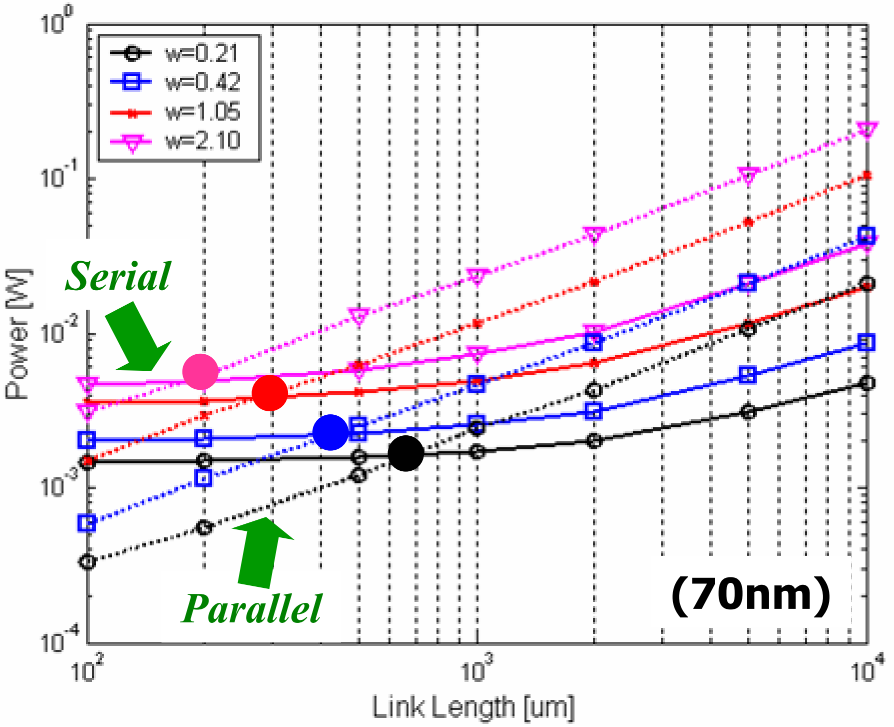
rce

er

Power parallel vs. serial link

Power vs. Wire Length

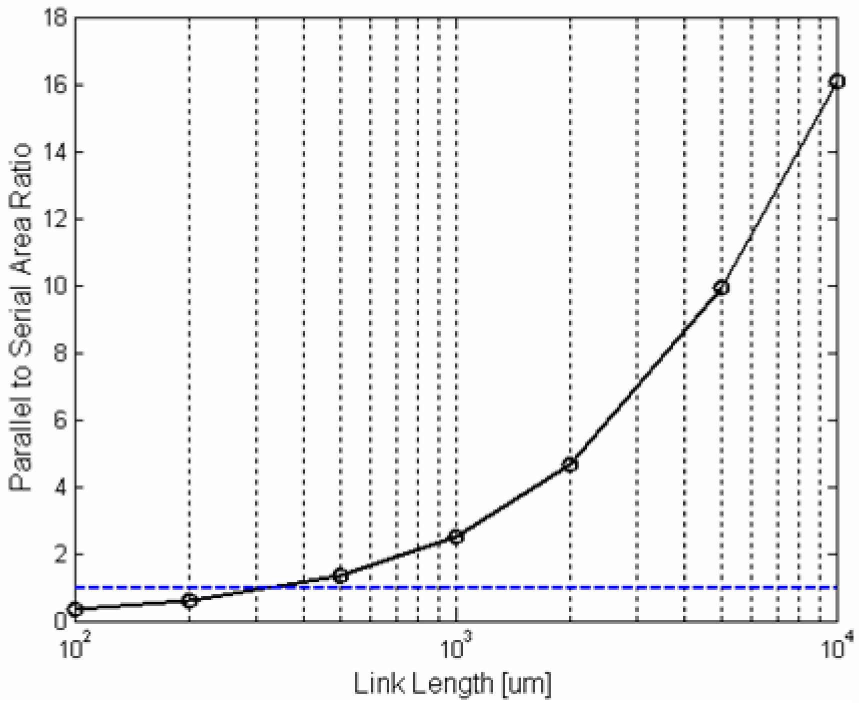




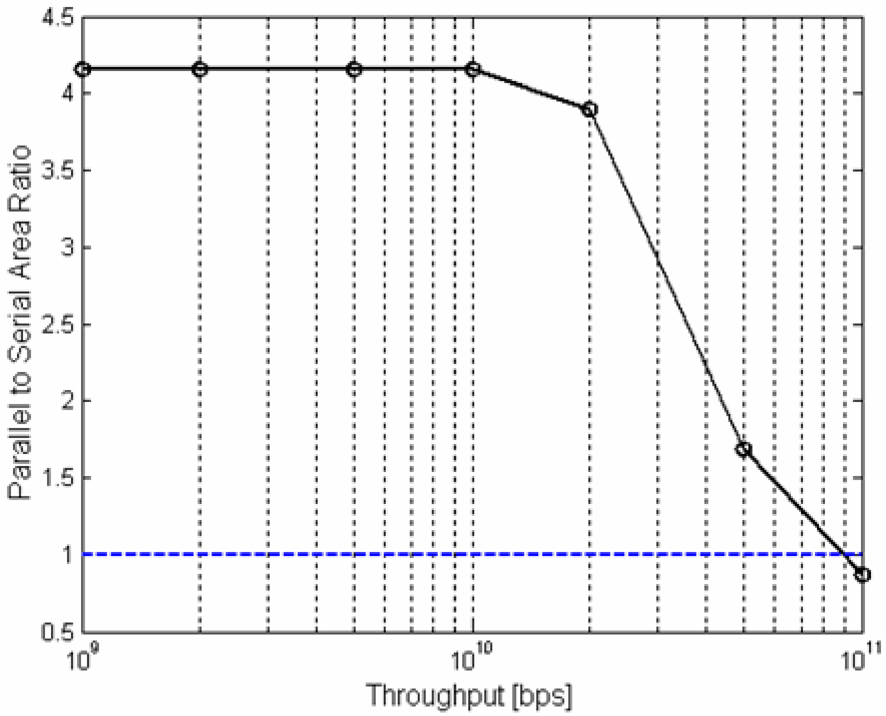
The benefit of Serial link in 70nm is more pronounced than in 130nm because of increased leakage current of repeaters in the parallel link

Area of parallel vs. serial link

Area vs. Wire Length

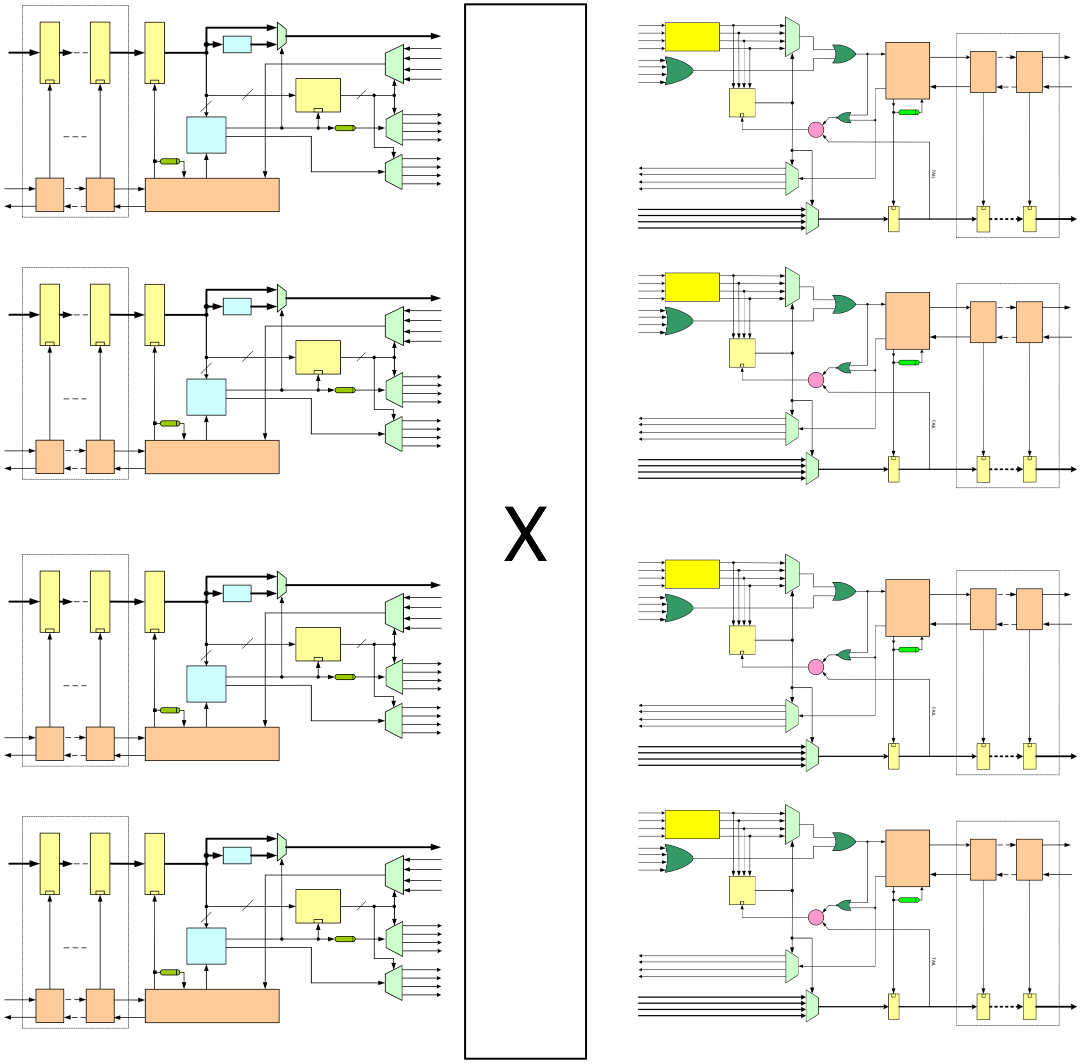


Area vs. Throughput



Serial link consumes lower area for long wires, where the area of serializer is not dominant, and throughput is achieved without excessive device sizing

Asynchronous Router



Optional Buffering

Di

Lb

Lb

D

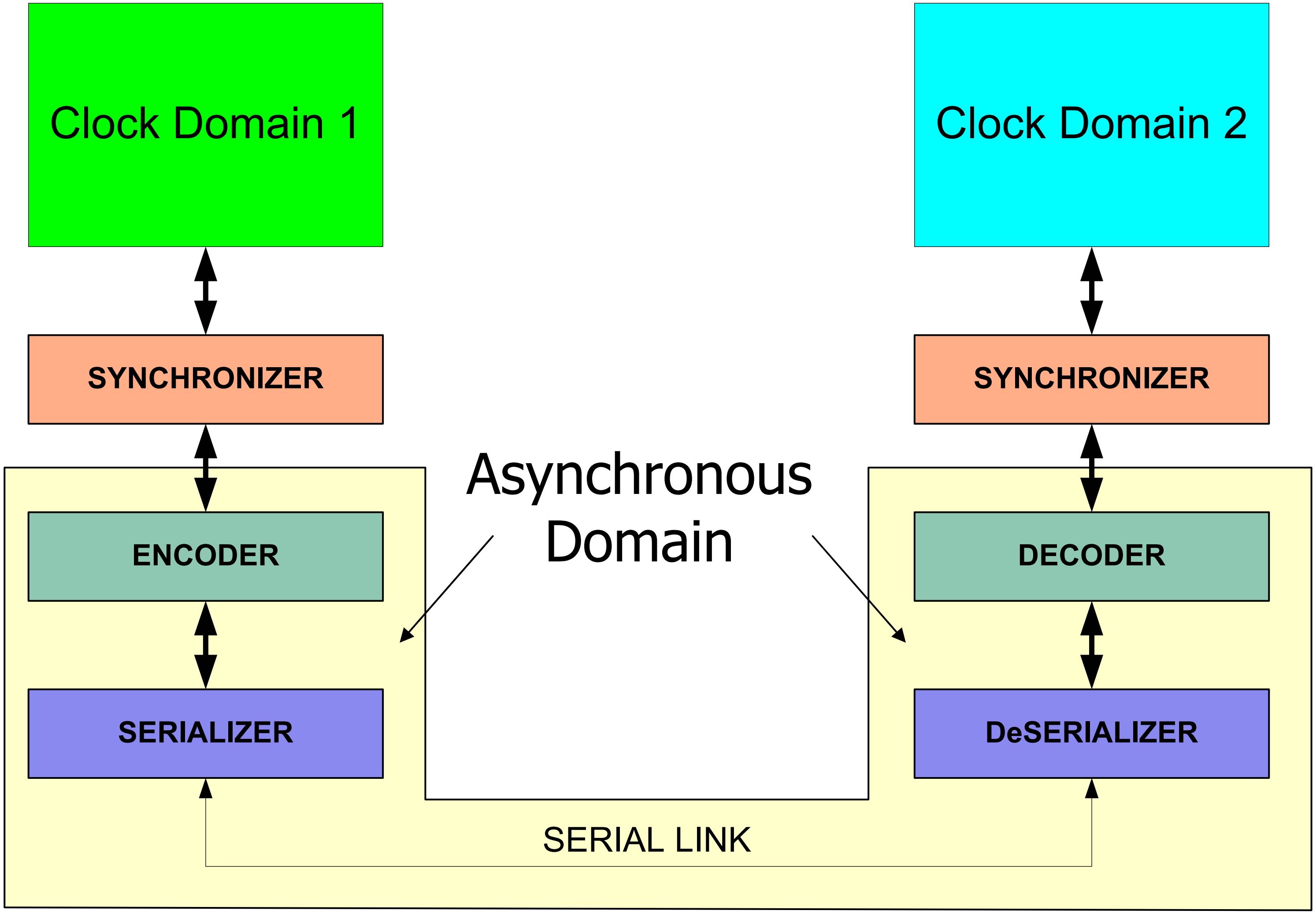
Ri

Ri

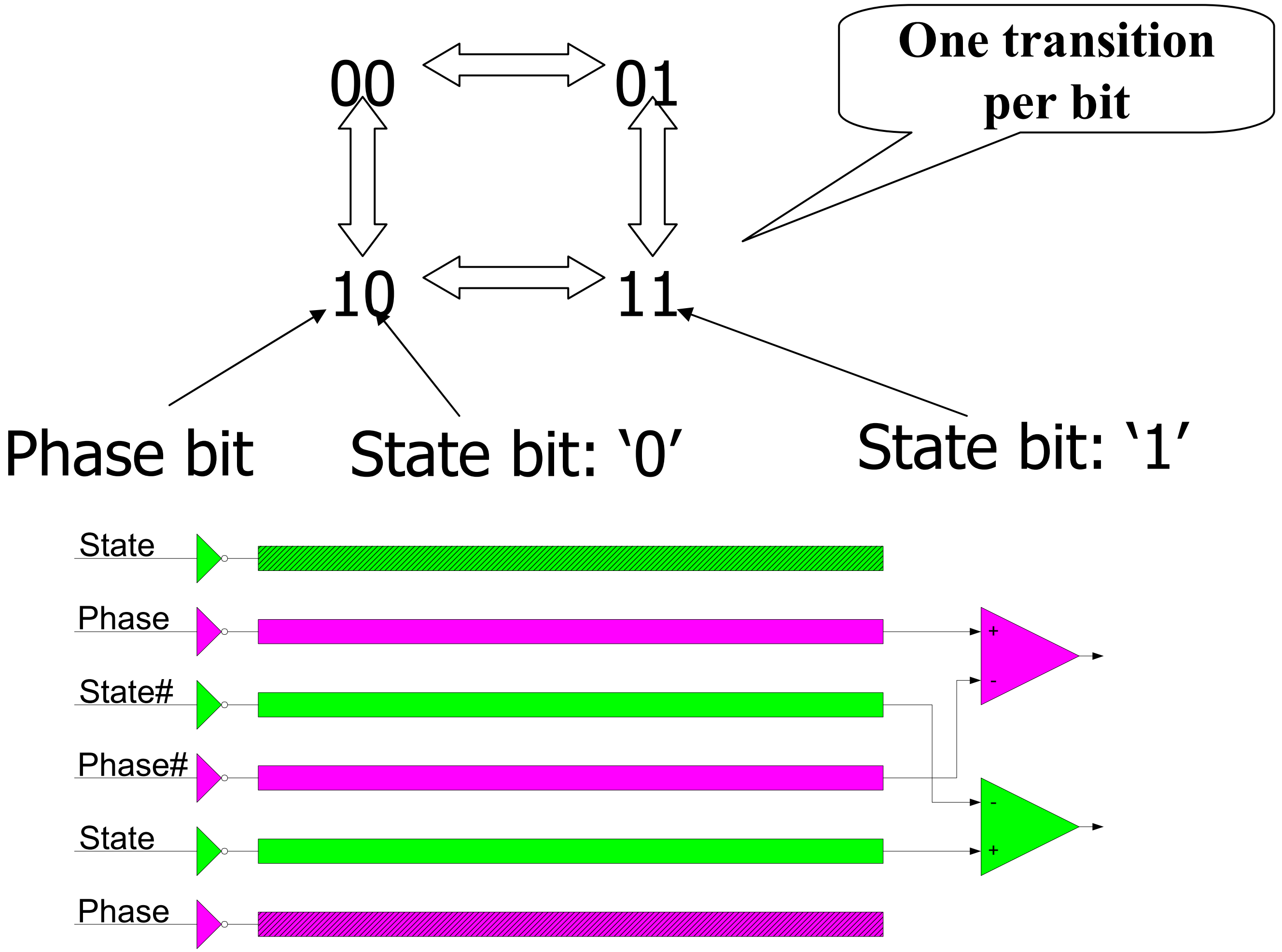
Ri

Solves synchronization, clock domain crossings, timing, long connects

High speed asynchronous serial links



Phase and State dual-rail encoding



One transition per bit

Phase bit

State bit: ‘0’

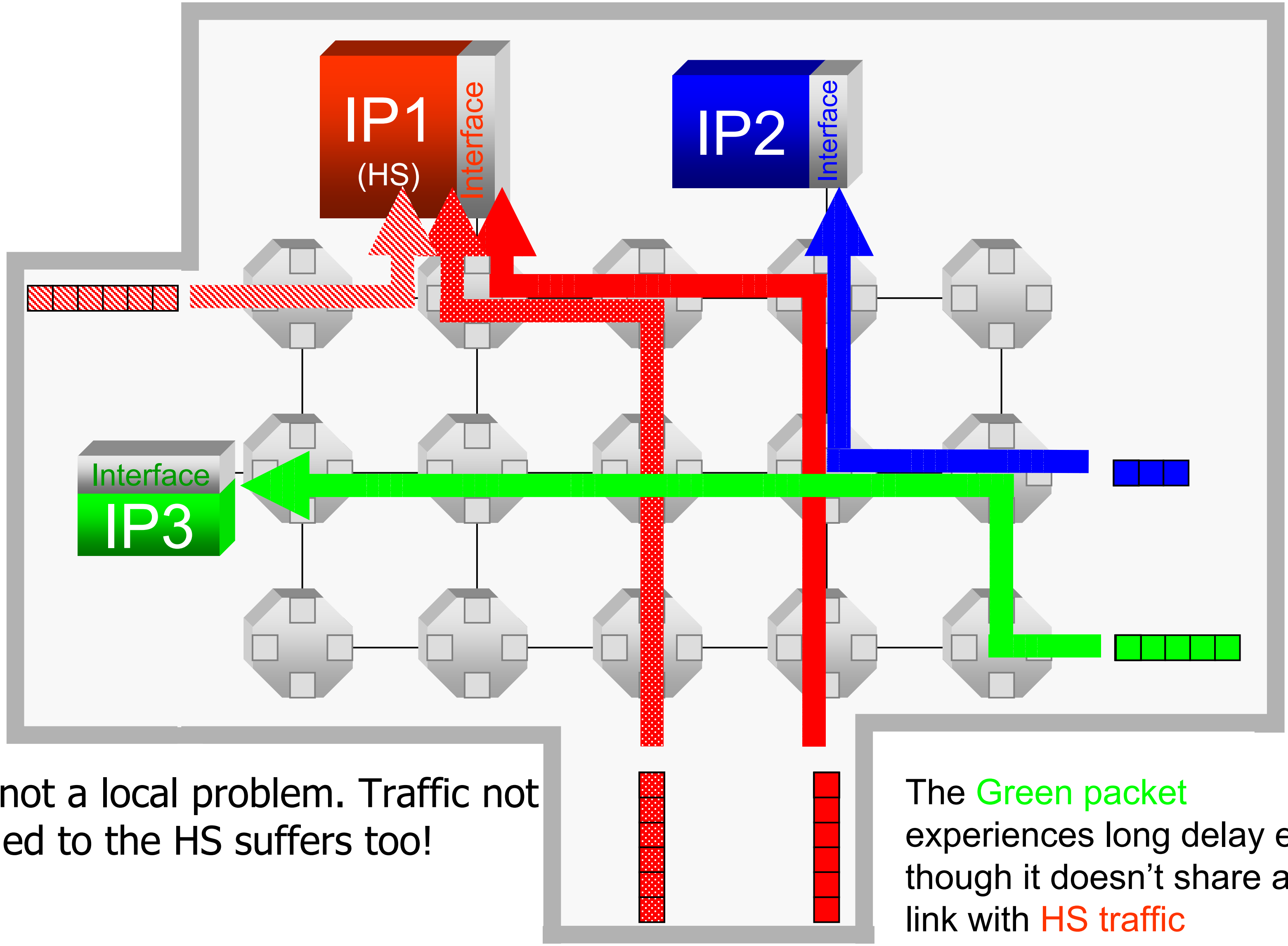
State bit: ‘1’

- “Self shielding” : Only one differential pair switches

Presentation Outline

- Research motivation
- Results of 2004
- **Future work**
  - **Hot-Spots**
  - **Latency-sensitive connections**

HotSpot in NoC

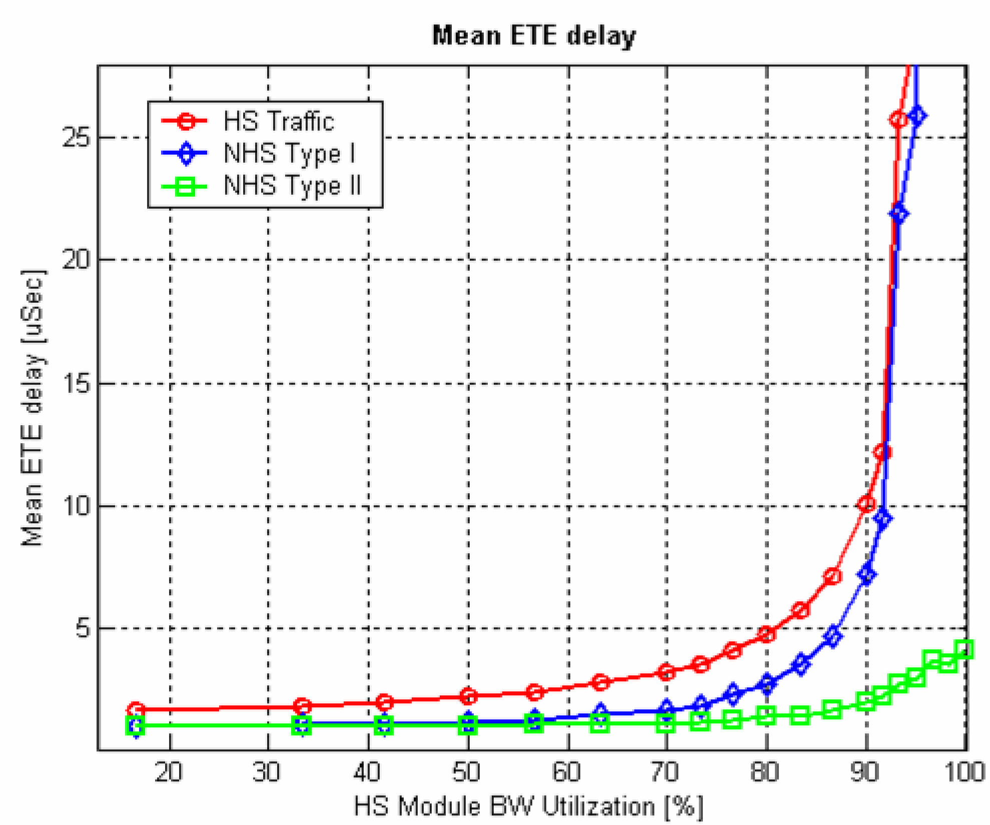


- HS is not a local problem. Traffic not destined to the HS suffers too!

The Green packet experiences long delay even though it doesn't share any link with HS traffic

Source fairness problem

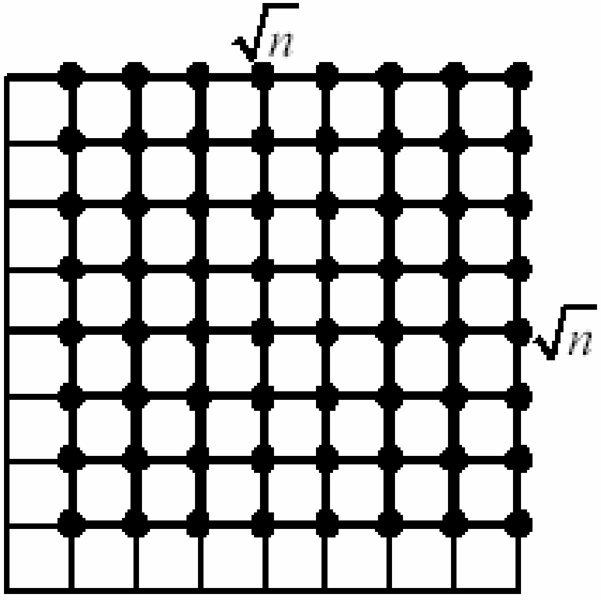
- QNoC routers are designed to be simple
  - Fast, low-area and power efficient
  - But cannot assure fair sharing of system's modules
- Instead, a simple end-to-end flow-control mechanism can be applied



NoC for Latency-Sensitive Communication

The Problem:

Low Latency is crucial for urgent data



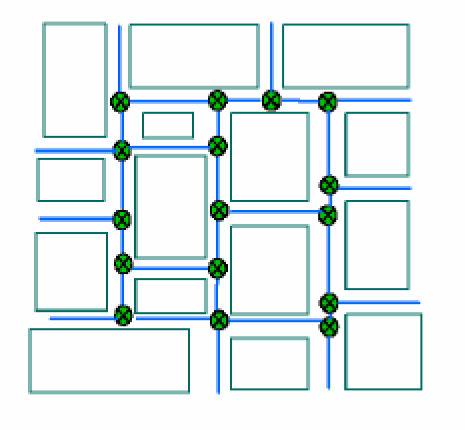
In Mesh:

Latency can reach many hop cycles!

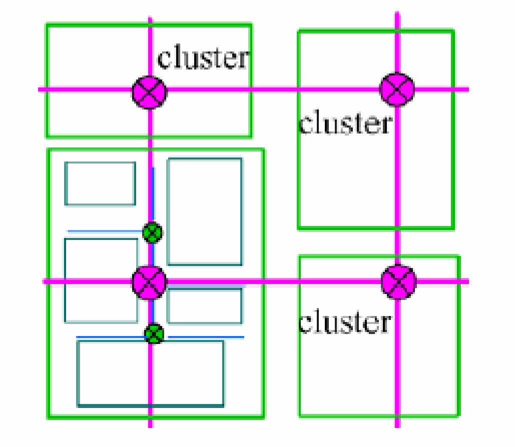
NoC for Latency Sensitive Communication

Hierarchical solution approach :

Irregular Mesh:



Hierarchical Mesh:



- ✓ Where to add such express links
- ✓ Performance improvements vs. cost

Summary

- Develop the QNoC design paradigm:
  - Architecture
  - Links
  - Circuits
  - Design flows & tools

- Start to investigate NoC-based multiple-core processors, as a proof-of-concept.

Backup – Mean Delay Equations

- Simple M/M/1 model: $t_j^i = \dfrac{1}{\frac{1}{l} \cdot C_j - \Lambda_j^i}$

  (mean flit interleaving delay of flow i on link j)

- Accounting for inter-link dependencies:

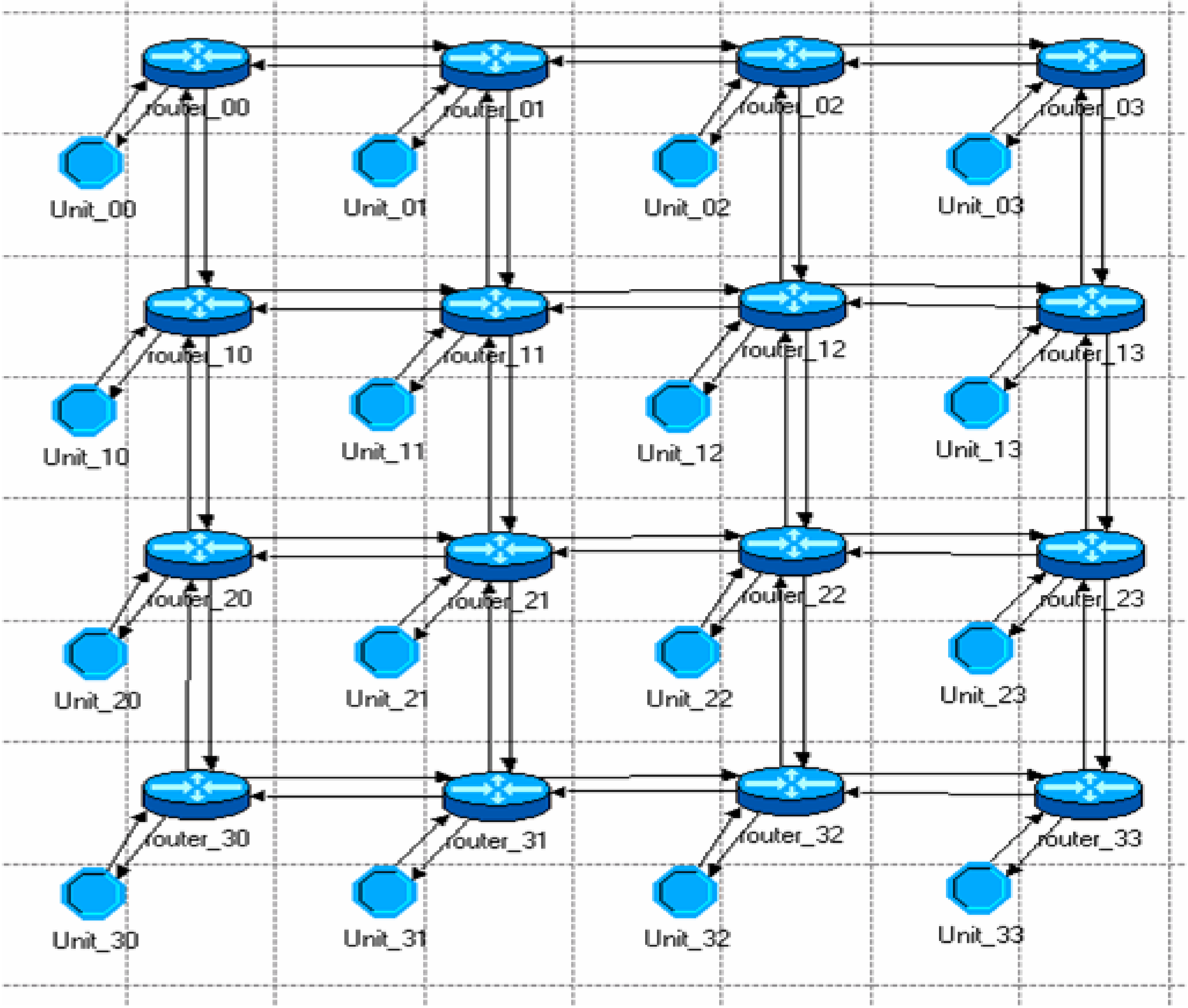
$$\tilde{t}_j^i = t_j^i + \sum_{k \mid k \in \pi_j^i} \frac{BW_k^i}{C_k} \cdot \frac{t_k^i}{dist^i(j,k)}$$

  (flit interleaving delay is affected by the delay in subsequent hops weighted by their utilization and distance)

- The total transfer time is dominated by the hop with the lowest service rate:

$$T^i \simeq \frac{l \cdot m^i}{\max(\tilde{t}_j^i \mid j \in \pi^i)}$$

4-by-4 System


router_00
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