Journal of Circuits, Systems, and Computers
Vol. 14, No. 3 (2005) 515–532

World Scientific
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COMPARISON OF SIGMA–DELTA CONVERTER CIRCUIT ARCHITECTURES IN DIGITAL CMOS TECHNOLOGY

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Received 3 May 2004
Revised 23 September 2004

Integration of analog-to-digital signal conversion circuits into digital submicron silicon chips is required for many applications. This is typically implemented by sigma–delta circuits, which can provide good resolution without requiring trimming of component values. This paper presents an analytical comparison of noise performance in four alternative sigma–delta circuit configurations which have been presented in the literature, consisting of discrete-time and continuous-time integration in voltage-mode and in current-mode. For high resolution, superiority of switched-capacitor circuits over the alternatives is shown, based on process technology considerations. Design guidelines are outlined for selecting oversampling rate and other key parameters, in order to obtain maximal data resolution.

Keywords: Analog–digital conversion; sigma–delta modulation; signal-to-noise analysis; low voltage CMOS; switched capacitors; switched current.

1. Introduction

VLSI technology scaling enables realization of complete electronic systems on a single silicon die. While such systems are primarily digital, some essential functions must be implemented as analog circuits. For example, a PC-on-a-chip would need integrated A/D conversion for audio signals, D/A conversion for video RGB outputs, etc. In the past, traditional system partitioning assigned these functions to separate chips, such that process technology optimized for analog circuits could be employed in their implementation. However, the economic drive towards low-cost, small-size systems suggests a shift in partitioning, and presents the challenge of implementing analog functions on the same chip with the rest of the system, using scaled CMOS technology, optimized for digital circuits and low voltage supply.[1]

This paper compares CMOS circuit architectures for sigma–delta A/D converter design. As an example, we use specifications that could be applied in a single-chip PC, providing 14-bit resolution at 20 kHz bandwidth in accordance with AC-97,[2] and 0.13 μm digital CMOS technology.[3] The analysis focuses on choice of the most suitable circuit topology among four types of circuits presented in the literature.

A sigma–delta converter[4] is the typical choice for this application, due to its ability to exploit high-speed oversampling, achieving high resolution while using low-complexity circuitry, and because of its tolerance to device mismatch and other circuit imperfections. Previous investigations have demonstrated high resolution in sigma–delta audio converters using supply voltages above 1.5 V, using technologies of 0.35 μm or previous generations.[5–12] Resolutions of 9–10 bits were demonstrated with supply voltages around 1 V.[13–16] The investigation of Ref. 17 achieved 14.9 bit resolution at 1.2 V, using a specialized 0.5 μm process. The published designs include both continuous time[11] and switched-current circuits[16] besides switched-capacitor implementations. Hence, combining discrete-time or continuous-time with current-mode or voltage-mode, there are four basic alternative circuit architectures to choose from. However, there is no rigorous comparison of the attainable resolution inherent to these circuit types. Most investigations focused primarily on low-power and low supply voltage for battery operation, although their process technology was designed for higher operating voltages. In such cases, the threshold voltage as a fraction of supply voltage is disproportionally large, and there is insufficient overdrive to turn on the transistors used as switches. To cope with the switch-driving problem, techniques such as voltage multiplication and switched op-amp[5,13,14] have been used.

This paper deals with a different set of goals and constraints: it uses a 0.13 μm CMOS process optimized for digital speed, with a threshold voltage of 0.3 V such that switch-driving is feasible with 1 V operating voltage. Ultra-low power is not essential, such that very high oversampling rates may be possible. On the other hand, intrinsic analog gain of the transistors is degraded with scaling. Within this framework, there are several design alternatives and choices to explore with regard to process parameters and limited voltage range, including integration order, oversampling ratio, discrete time versus continuous time operation, and choice of current versus voltage signal (switched-capacitors versus switched-current circuit architecture).

Section 2 of this paper presents the four basic circuit options and describes a system-level analysis and simulation of the above issues, yielding several possible combinations of integration-order and oversampling ratio. However, the system-level analysis ignores circuit-specific noise and error sources. Section 3 comparatively analyzes circuit noise and error sources in the four basic alternative circuit topologies. Section 4 discusses design considerations based on technology parameters, combining the results of analysis at the system-level and at the circuit-level.

2. Circuit Topology Choices and System-Level Analysis

Sigma–delta converters[18–21] use oversampling and noise shaping to achieve high-resolution output, while using a simple quantizer. Sigma–delta circuit topologies reported in the literature can be classified by the choice of signal (voltage or current signal at the integrator) and by the type of integrator used (discrete-time or continuous-time). Figures 1–4 present the four basic combinations of a first-order single-ended modulator. Discrete-time voltage mode circuits are often denoted by the acronym SC (switched capacitor),[6,8] and discrete-time current-mode circuits are denoted by SI (switched current).[16] In discrete-time modulators (Figs. 1 and 2), sampling is done at the input of the modulator. In continuous time modulators[11] (Figs. 2 and 4), the integrator works continuously and sampling is done at the quantizer, after the integrator.

In a standard digital process, the switched capacitors must be implemented by a sandwich structure of metal layers.[22] Current-mode circuits seem to have an advantage because they may allow signals to span a large range of currents, in contrast with the limited signal range (dictated by supply voltage) in voltage-mode circuits.[23] The switched-current topology is also interesting, in particular because it does not require any special capacitors.[24] Hence, the choice of a basic circuit topology and consequent design parameters is not obvious.

In any circuit-option, a single-bit quantizer (simple comparator) would be best, due to its inherent linearity and tolerance to device mismatches.[18] Additional design decisions, which must be made, include the order of integration L and the oversampling ratio M. These parameters determine the transfer of quantization noise

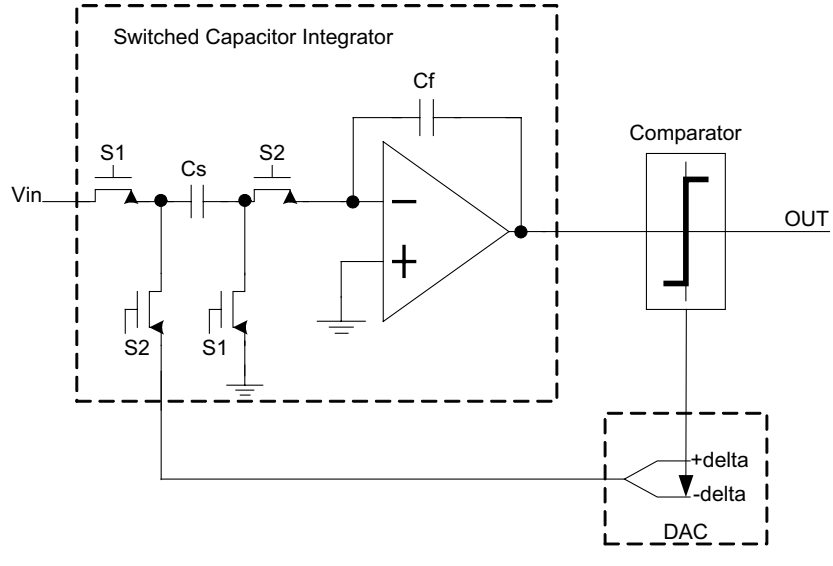

Fig. 1. First-order single-ended switched capacitor sigma–delta modulator. Sampling capacitor C_S is a linear floating capacitance.

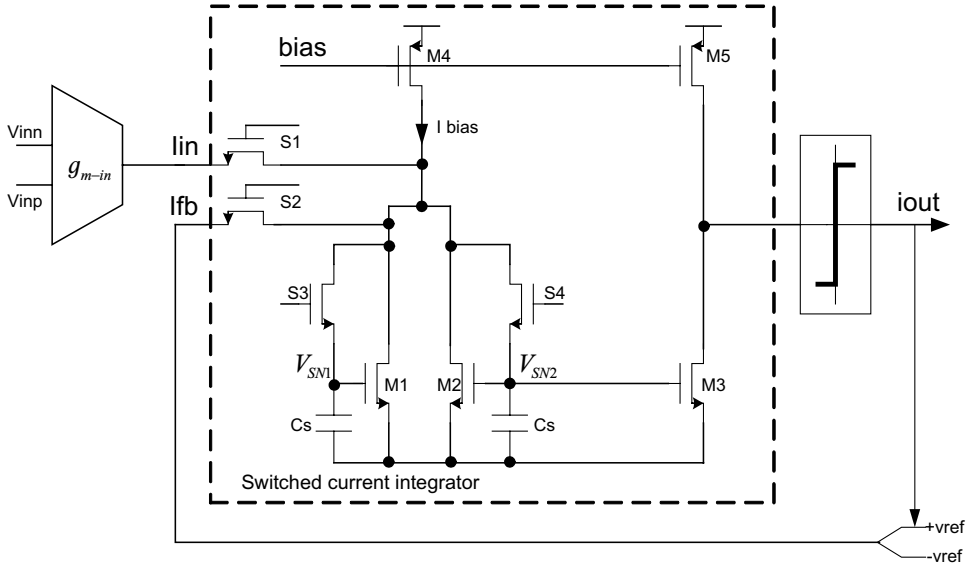

Fig. 2. Switched current modulator. Sampling capacitors C_S are MOS transistor gate capacitances.

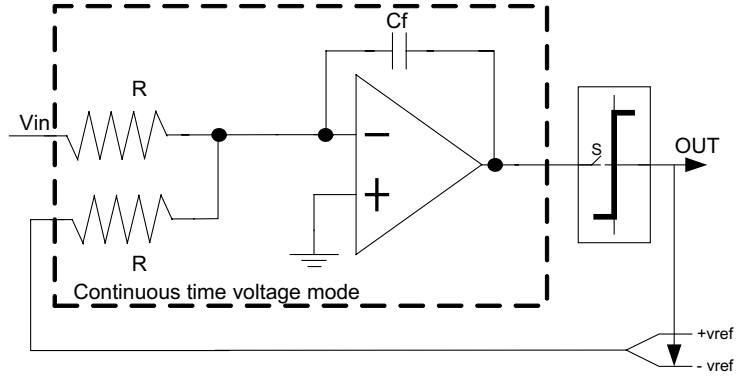

Fig. 3. Continuous time voltage mode modulator. Sampling is performed in the quantizer.

into high frequencies beyond the signal band, such that it can be filtered out in the digital domain. If the quantization error were the only problem, the signal-to-noise ratio in any of the circuits would be given by Eq. (1) with the number of quantizer bits $n = 1$, assuming a sinusoidal input signal and using the well-known white-noise approximation for the quantization error[25]:

$$\text{SNR } [dB] = 6.02n + 1.76 + 10 \log \left[\left(\frac{M}{\pi} \right)^{(2L+1)} \pi(2L+1) \right] . \tag{1}$$

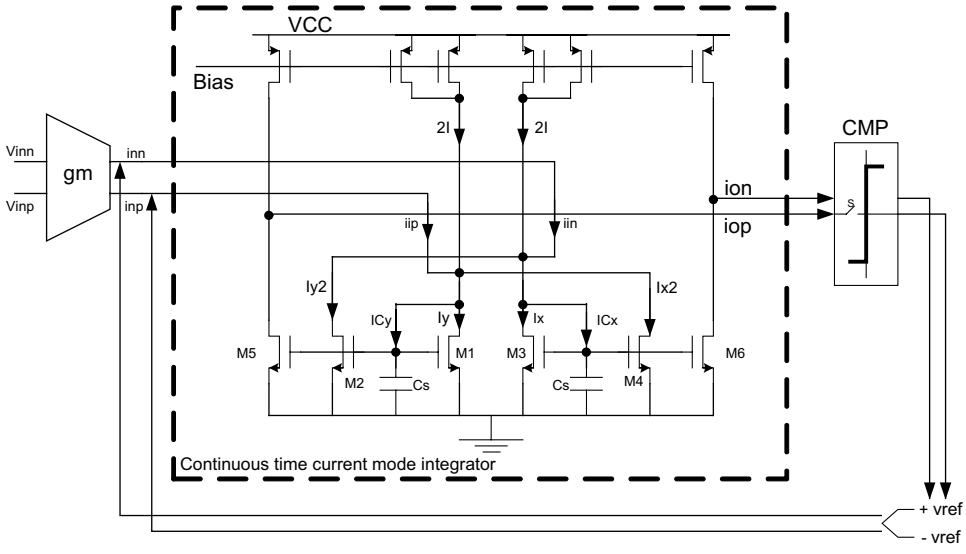

Fig. 4. Continuous time current mode modulator. A differential sampling quantizer is used.

In practice, the real signal-to-noise performance of such circuits depends on additional error-sources, noise mechanisms and circuit imperfections. These are affected by the choice of circuit topology, integration order, and oversampling ratio. The purpose of our study is to analyze and compare limitations of each circuit topology, show the effects of circuit and process parameters on the achievable SNR, and explore possible design tradeoffs.

System-level considerations can help to narrow down the design options. First, we rule-out first-order integration, because first-order sigma–delta converters are too vulnerable to idle tones,[26] an inherent imperfection of the sigma–delta architecture which is tolerable at second-order and above. Instability is another problem, which exists at third-order and above. Hence, it would be desirable to utilize stable second-order integration ($L = 2$), and achieve the desired signal-to-noise ratio by a high M. Alternatively, if 3rd- or 4th-order is required, stability can be achieved by gain scaling in the integrators[27,28] or by cascading first-order integrators, which are inherently stable.[29] Both these approaches expose the modulator to analog cell imperfections such as amplifier offset and high sensitivity to finite DC gain in the amplifier.[29] Although the 2nd-order option looks more promising for a fast digital process with rather poor analog cells, the choice between these alternatives must depend on circuit-specific noise analysis, which might impose limits on usable values of M. This analysis will be presented in Sec. 3.

Another limit on the oversampling ratio M stems from "integrator leakage", which is actually due to finite DC gain of amplifiers (note that ideal integrators require amplifiers that have infinite gain at zero frequency).[24,30] System-level analysis shows that practical integrators, which are "leaky", transfer more low frequency

elements of the quantization noise that will not be filtered by the digital low-pass filter and are more sensitive to idle tones,[31] and therefore will reduce the modulator's performance. To minimize this performance reduction, the amplifier's dominant pole must be much lower than signal bandwidth, such that the DC gain A of the amplifier becomes much larger than M[25]:

$$A > \frac{M}{\pi}\,. \tag{2}$$

System-level behavioral simulation results for a second-order sigma–delta modulator with sinusoidal input at 20 kHz are shown in Fig. 5. The model was written in Matlab using a methodology similar to Ref. 32, and its time-domain results were converted to the frequency domain. Besides quantization noise, the behavioral model also accounts for integrator leakage, comparator offset, stage gains, output saturation and idle tones. The model was used to specify and optimize some parameters (for example, stage gains of 0.5 were chosen). Simulation results show that our specification is realizable, unless circuit-specific noise becomes dominant. Such circuit-level noise analysis is the topic of the next section.

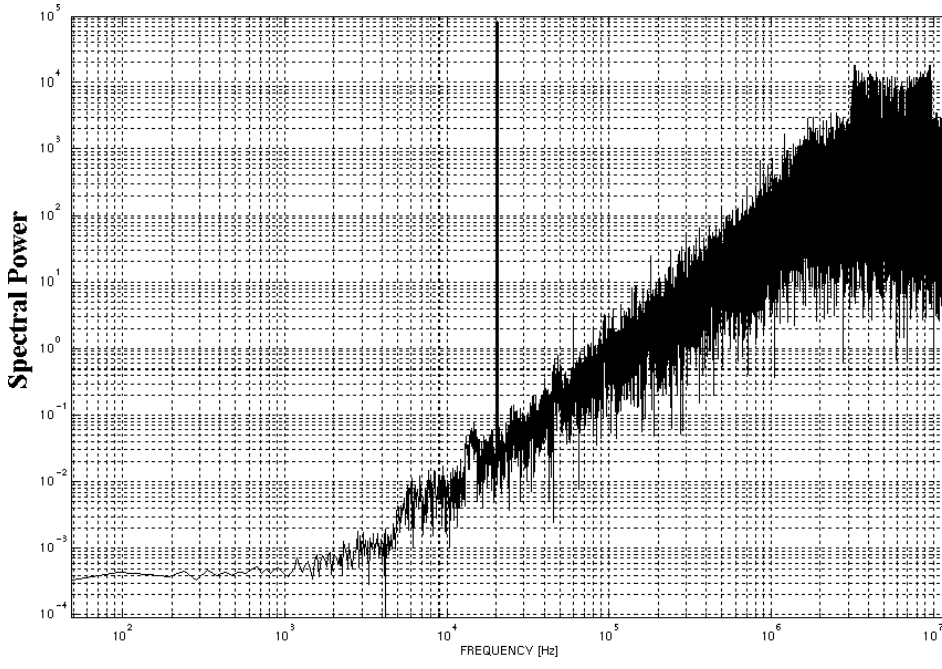

Fig. 5. Power density of a second-order sigma–delta modulator with sinusoidal input at 20 kHz, obtained from time-domain behavioral simulation, converted by FFT. The model accounts for shaped quantization noise, integrator leakage, comparator offset and output saturation. Oversampling ratio is 256, the extracted signal-to-noise ratio is SNR = 101 dB assuming an ideal digital low-pass filter.

3. Comparison of the Four Basic Circuit Topologies in Terms of Noise Performance

We use the approach of Ref. 33 to compare various noise and error sources in each circuit topology. All error sources in the system are regarded as noise. Some error sources in the circuit are correlated with the input signal, and hence distortion analysis should be employed. However, we assume that the nonlinear quantization and the feedback in the circuit causes de-correlation, effectively converting the error into white-noise, and thus we use the white-noise approximation for all error sources. We present each noise term as a function of oversampling ratio. The simplicity of this method will enable us to compare the salient characteristics of noise behavior in the four basic circuits, analyze the contribution of each noise source to the total within each circuit, and draw appropriate design conclusions.

3.1. *Analysis of 1-bit switched capacitor (SC) sigma–delta modulator*

The operation of this circuit (Fig. 1) is described in Ref. 20. The noise sources are as follows:

(1) Quantization noise[18] is given by:

$$V_{q-SC}^2 = V_{pp}^2 \left(\frac{1}{M}\right)^{(2L+1)} \frac{1}{48} \frac{\pi^{2L}}{(2L+1)}, \tag{3}$$

where V_{pp} is the maximum input voltage signal-swing (peak to peak), L is the integrator order and M is the oversampling ratio.

(2) Thermal noise originating from switches at the sampling capacitor C_S and the input stage[33] is given by:

$$V_{th-SC}^2 = \frac{1}{M} \frac{kT}{C_S} \left[2 + \frac{4}{3}\left(1 + \frac{\alpha}{g_m}\right)\right] \approx \frac{4}{M} \frac{kT}{C_S}, \tag{4}$$

where k is the Boltzman constant, T is the absolute temperature, g_m is the amplifier transconductance, C_S is the sampling capacitor and α is a factor that depends on the amplifier configuration.[33] From Eq. (4), we see that the thermal noise can be reduced by increasing M or C_S. Each doubling of the oversampling ratio or of the sampling capacitor reduces the thermal noise by 3 dB. Unlike quantization noise, thermal noise is not affected by the integrator order L.

(3) Settling noise, originating from incomplete transition of the integrator's output at the end of the clock phase, due to bandwidth and slew-rate limitations. Assuming that the settling error is uncorrelated with the input signal and uniformly distributed, the settling noise is[33]:

$$V_{set-SC}^2 = K_{\text{int}} \frac{1}{M} e^{-g_m/2f_0 MC_s}, \tag{5}$$

where

$$K_{\text{int}} = \frac{1}{3}\left(\frac{I_{SR}}{g_m}\right)^2 \left(1+\frac{C_S}{C_f}\right)^2 e^{2((V_{PP}(C_S/C_f)g_m)/(I_{SR}(1+(C_S/C_f)))-1)},$$

f_0 is the input bandwidth, C_f is the feedback capacitor in the integrator, and I_{SR} is the slew rate current of the amplifier.

From Eq. (5), we see that the settling noise depends on the oversampling ratio M in two different ways. First, the factor $1/M$ describes averaging of the noise by oversampling (assuming a low-pass filter in the digital domain). Second, the exponential factor grows steeply as we reduce the time slot available for settling of the integrator's output signal.

(4) Jitter noise, reflecting errors due to inaccurate sampling time caused by random variations in the clock waveform.[20] Assuming an uncorrelated random process with maximum jitter $\Delta t_{\max}$, we obtain

$$V_{jt-SC}^2 = \frac{V_{pp}^2}{12}\frac{(2\pi f_0 \Delta t_{\max})^2}{M}. \tag{6}$$

Dependence on whether M is the same as for thermal noise: each doubling of the oversampling ratio reduces the jitter noise by 3 dB.

In this analysis, we neglect clock feed-through noise, which exists in switched capacitor circuits but can be reduced by circuit techniques (such as bottom-plate sampling and low injection switches[34]) and has very little effect on signal-to-noise ratio. We also neglect $1/f$ noise and the impact of amplifier nonlinearity.

In Fig. 6, all noise contributions for second-order switched capacitor topology are plotted versus the oversampling ratio, using a set of technology parameter values given in Table 1.

There are three regions in Fig. 6: First, at low oversampling ratios, quantization noise dominates. Second, at middle frequencies, thermal noise dominates. Third, at high sampling rates, settling error is the dominant noise. In the given technology, jitter noise is negligible for SC circuits. The maximum achievable resolution is located in the second region where total noise is minimal and thermal noise is the limiter. Trying to improve the SNR by using higher order of integration will have no effect since thermal noise and settling error are not dependent on L. This is not the case for the oversampling ratio, which reduces thermal noise. This conclusion supports the choice that we made in the system analysis — preferring lower integration order and higher oversampling ratio.

3.2. *Analysis of 1-bit switched current (SI) sigma–delta modulator*

The operation of this circuit (Fig. 2) is described in Ref. 23. Although the integrator uses current as input signal, comparison is easier if we assume that the input of the system is voltage. Hence, for the sake of comparison, we assume an ideal voltage to current converter with transconductance g_{m-in} at the input, and we multiply

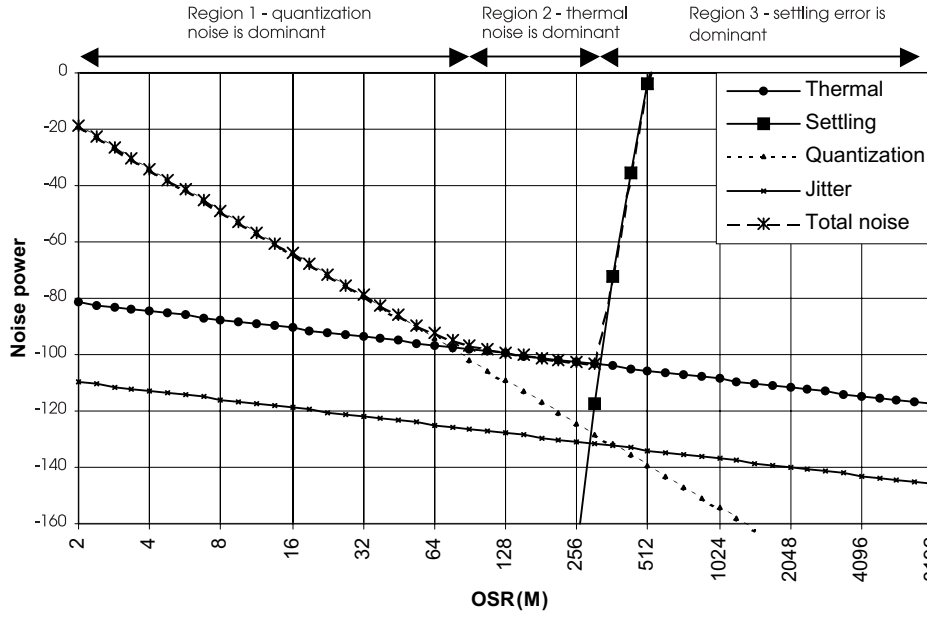

Fig. 6. Noise components in a second-order switched-capacitor sigma–delta modulator as a function of the oversampling ratio M. Thermally limited operation is achieved in the middle region ($128 < M < 256$); settling noise becomes dominant at higher sampling frequencies.

all noise components by the inverse transfer function $(1/g_{m-in})^2$. Note that in practice, such voltage-to-current conversion might not be possible at sufficiently high resolution.

Following Ref. 23, the noise components are as follows.

(1) Quantization noise is given by Eq. (3), with $V_{pp} = I_{pp}/g_{m-in}$, where I_{pp} is the maximum input current signal swing (peak to peak).

(2) Thermal noise is given by[23]:

$$V_{th-SI}^2 = \frac{g_{m0}^2}{g_{m-in}^2} \frac{1}{M} \frac{kT}{C} \frac{2}{3} \left(1 + \frac{g_{mj}}{g_{m0}}\right), \tag{7}$$

where g_{m0} represents the transconductance of transistors $M1$, $M2$ and g_{mj} represents the transconductance of the bias transistor $M4$. The dependence of thermal noise on the oversampling ratio is similar to that of a switched capacitor integrator in Eq. (4). The additional coefficient g_{m0}^2/g_{m-in}^2 reflects the ratio between the input signal voltage swing and the voltage swing at the sampling nodes (V_{SN1}, V_{SN2}). Since the voltage swing at a sampling transistor's gate is much smaller than V_{PP}, the ratio g_{m0}^2/g_{m-in}^2 leads to higher thermal noise in switched current topology than in switched capacitor modulators. Thus, the advantage of this circuit topology (it does not require special large-area sampling capacitors) comes together with an inherent disadvantage in terms of noise.

Table 1. Parameters for all circuit topologies.

Parameter	Typical value	Units	Description
n	1		Number of bits
V_{pp}	1	[V]	Maximum input voltage signal swing (differential peak to peak)
V_{CC}	1	[V]	Supply voltage
f_0	25	[kHz]	Input bandwidth
C_{OX}	1.5e−2	[F]	Transistor oxide capacitance, $C_{ox} = \varepsilon_0 \varepsilon_{ox}/t_{ox}$, process dependent
$\Delta t_{\max}$	50	[ps]	Clock jitter — maximum value
g_m	5	[mS]	Amplifier transconductance
C_S	1	[pF]	Sampling capacitor is chosen to reduce the thermal noise at oversampling ratio of 256 to the needed level
C_f	4	[pF]	Feedback capacitor is chosen to achieve integrator gain of 2
I_{SR}	0.3	[mA]	Slew Rate current
Δ	0.5	[V]	Maximum input voltage step
g_{m0}	2	[mS]	Sampling transistor transconductance
g_{mJ}	4	[mS]	Bias transistor transconductance
I_{pp}	0.2	[mA]	Maximum input current signal swing (peak to peak)
g_{m-in}	1	[mS]	Input voltage to current transconductance
i_{bias}	0.4	[mA]	Bias current of the sampling transistor
W, L	16, 1	[μm, μm]	Sampling transistor size (Width and Length)
W_J, L_J	32, 1	[μm, μm]	Bias transistor size (Width and Length)
W_n, L_n	0.4, 0.13	[μm, μm]	NMOS switch transistor size (Width and Length)
W_p, L_p	0.4, 0.13	[μm, μm]	PMOS switch transistor size (Width and Length)
λ	0.005	[V^{-1}]	MOS transistor short channel effect factor
R	2	[kΩ]	Integrator serial resistor value

(3) Settling noise: Using the expression developed by Nairn[35] for the step response of a current mirror and using the white-noise approximation, it is possible to derive the following error expression for settling noise in SI circuit:

$$V_{set-SI}^2 = \frac{3}{g_{m-in}^2 M} \left[5 I_{PP} \frac{X_{\max}}{1 + X_{\max}^2} \right]^2 , \tag{8}$$

where

$$X_{\max} = \frac{1}{6} e^{-\sqrt{5 I_{PP} \beta}/2 f_0 M C} ,$$

$$\beta = \mu_0 C_{OX} \frac{W}{L} .$$

Assuming $I_{PP} = 1/2 I_{\text{bias}}$, where i_{bias} is the bias current and I_{PP} is the maximum peak-to-peak input current. This result has high similarity to the settling expression in SC topology (5).

(4) Clock feed-through error is caused by nonlinear injection of charge to the sampling capacitor when the switch transistors are closed. Using the analysis made by Dias for current error[36] and applying the white-noise approximation, it is possible

to derive the feed-through error expression:

$$V_{CFT-SI}^2 = \frac{1}{3Mg_{m-in}^2}\left\{K\left[\left(\frac{C_{SW}}{C_S}+1\right)\left(\sqrt{\frac{3I_{PP}}{K}}+V_t\right)\right.\right.$$
$$\left.\left.+\Delta V_{OS}-V_t\right]^2-3I_{PP}\right\}^2, \tag{9}$$

where

$$K=\frac{1}{2}\mu_0 C_{OX}\frac{W}{L},$$

$$\Delta V_{OS}=\frac{C_{OX}}{C_S}\left[-\frac{1}{2}W_pL_pV_t-\frac{1}{2}W_nL_n\left(V_{CC}-V_t\right)+V_{DD}\left(W_pL_{OVL}-W_nL_{OVL}\right)\right].$$

The second component in Eq. (9) is dependent on the gate voltage and is presented using a coefficient C_{SW}/C, where:

$$C_{SW}=\frac{1}{2}C_{OX}(W_pL_p+W_nL_n).$$

From this analysis, we see that the clock feed-through error increases for higher values of the bias current. As in previous noise sources, the error is proportional to $1/M$. Design techniques that are used in switched capacitor (bottom plate sampling) are not applicable in the switched current topology and therefore the contribution of the clock feed-through error is much more significant.

(5) Finite output conductance error is caused by nonideality of the MOS transistor in saturation, leading to imperfect current-mirror operation. In switched current sampling, we assume that current in the transistor is determined only by gate voltage, regardless of the drain–source voltage. Since in practice, there is a dependency of i_{ds} on V_{ds} in saturation region, any change in V_{ds} from the sampling phase to the hold phase creates an error.

Using the expression for the current error that was developed by Dias[36] and using the white-noise approximation, the error expression is given by:

$$V_{FOC-SI}^2=\frac{1}{3M}\frac{1}{g_{m-in}^2}\left\{\left[\frac{3}{2}\lambda_1 I_{PP}+2\lambda_j I_{PP}\right.\right.$$
$$\left.\left.+2\theta\sqrt{3KI_{PP}}\right]\sqrt{\frac{I_{PP}}{K}}\left(\sqrt{3}-1\right)\right\}^2, \tag{10}$$

where

$$\theta=\frac{C_{dg1}}{C_{dg1}+C_{gs1}+C},$$

where λ_1 and λ_j are the short channel effect factor of the sampling transistor and the bias transistor, respectively.

From Eq. (10), we can see that the finite output conductance error depends on the bias current and on the output conductance of the transistor. When choosing higher values of bias current or transistors with lower output resistance, the finite output conductance noise will increase.

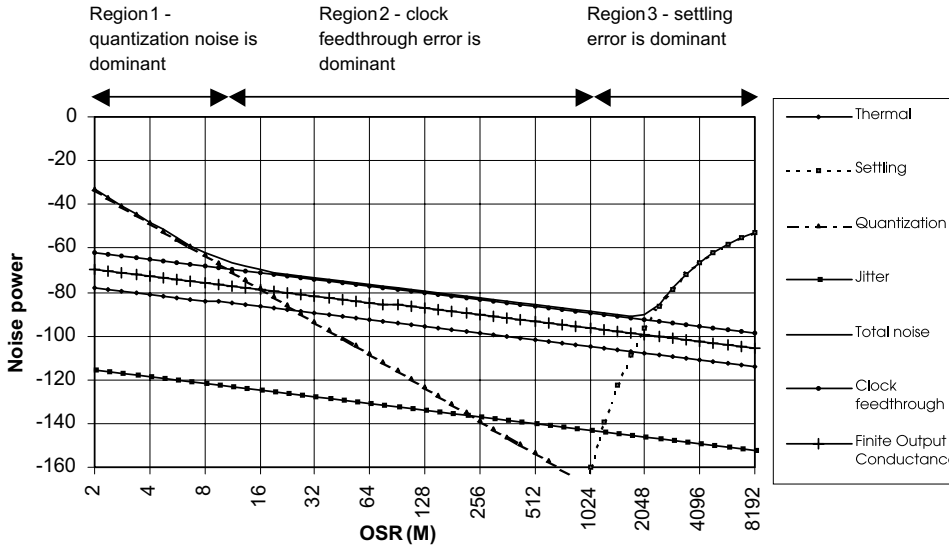

Fig. 7. Noise components in second-order switched current circuit topology. Clock feed-through and finite output conductance error dominate at middle frequencies. The useful range of oversampling ratio is limited by settling error.

(6) Jitter noise in switched current modulator: The analysis of jitter noise is equivalent to the one used for the switched capacitors modulator and the noise expression is given by Eq. (3), with $V_{pp}^2 = I_{pp}^2/g_{m-in}$.

All noise sources for second-order switched current topology are shown in Fig. 7, using the set of technology parameters given in Table 1.

Figure 7 has some similarity to the switched capacitor case. The three regions are dominated by quantization noise, clock feed-through and settling error, respectively. However, both clock feed-through and finite output conductance noise are higher than thermal noise in the middle region, reducing the maximum achievable SNR performance. In addition, the thermal noise has a higher value than in the case of switched capacitor because of low signal swing on the sampling transistor gate. The settling error has a lower value compared to switched capacitor, but still behaves as a limiter to the oversampling ratio for our application. As in SC topology, there is no benefit in moving to higher-order integration. Overall, achievable performance is lower than in switched capacitor topology, and does not meet the requirements for our specifications.

3.3. *Noise analysis of 1-bit continuous-time sigma–delta modulator*

For continuous time sigma–delta modulator, we analyze a voltage mode circuit. The results apply also for current mode continuous-time sigma–delta modulators.

The operation of this circuit (Fig. 3) is described in Ref. 18. Following Ref. 37, the noise sources are as follows.

(1) Quantization noise is described by Eq. (3).

(2) Thermal noise sources are the input resistor, feedback resistor and the equivalent input impedance of the amplifier. Since the frequency of the RC integrator pole is lower than the sampling frequency (by the oversampling ratio), noise is filtered by this RC filter and is not folded because of sampling. Accordingly, the total input thermal noise is dependent on the sampling frequency. The total thermal noise is given by[37]:

$$V_{th-CT-V}^2 = 2kTR_t(2f_0)\,, \tag{11}$$

where

$$R_t = 2R + \frac{4}{3}\left(1 + \frac{\alpha}{g_m}\right)\frac{1}{g_m}\,,$$

R is the resistance of the input resistor, g_m is the amplifier transconductance and α is a factor that depends on the amplifier configuration and its typical value is close to g_m.

(3) Jitter noise: In continuous time modulators, the jitter causes uncertainty in the time duration of the integration phase. This uncertainty translates into charge on the capacitor at the end of the integration phase. The expression for the jitter noise was derived in Ref. 37 and is given by:

$$\begin{aligned} V_{jt-CT-V}^2 &= \frac{8}{3}\Delta^2\Delta t_{\max}^2(2f_0)^2M\,, \\ \Delta &= \left(\frac{I_{fb}}{Cf}\right)\frac{T}{2}\,, \end{aligned} \tag{12}$$

where $\Delta t_{\max}$ is the peak value of the jitter, f_0 is the input signal bandwidth, I_{fb} is the feedback current, C_f is the feedback capacitor, T is the period of the sampling clock and Δ is the feedback voltage which is $V_{PP}/2$. Using this analysis, we can see that increasing M will increase the jitter noise.

All noise contributions for second-order continuous time voltage mode topology are shown in Fig. 8, using the same set of technology parameters.

Minimum noise power is achieved at the point where quantization noise and jitter noise are equal. Using a higher order, modulator will move this point to a lower value of oversampling ratio, where the jitter noise is smaller. This is valid as long as the jitter noise is higher than the thermal noise. To achieve 100 dB SNR, we need to use an oversampling ratio of less than 32. Using behavioral simulations, we have found that integration of at least 4th-order is required in this case.

4. Discussion

By comparing Figs. 6 and 7, it is evident that second-order discrete-time sigma–delta modulators are limited by quantization noise at low sampling frequencies,

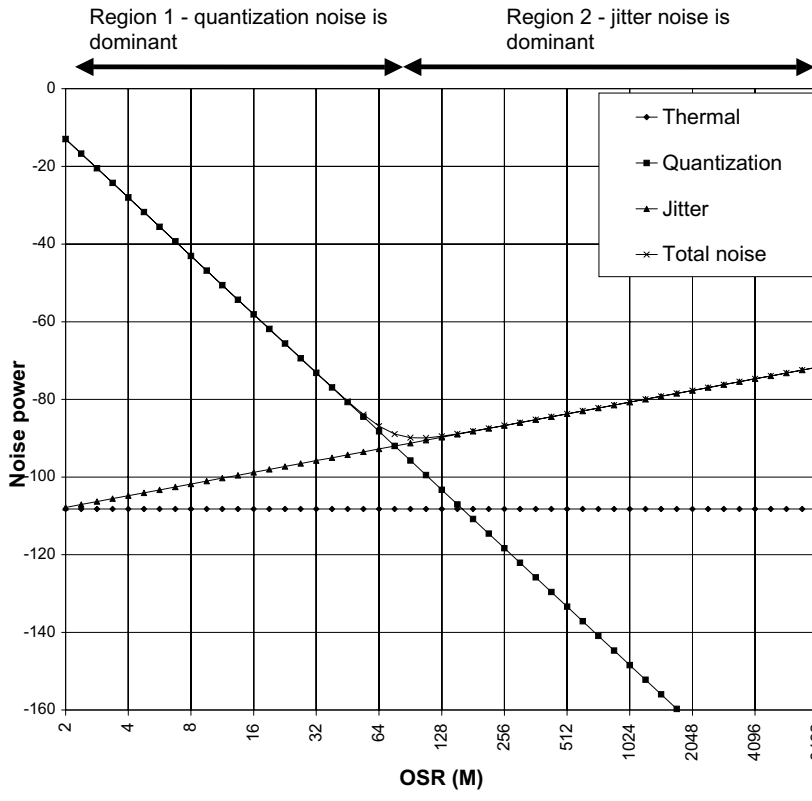

Fig. 8. Noise components in second-order continuous-time modulators. Clock jitter noise is dominant and it grows with increasing frequency. The minimum-noise point can be improved by using a low oversampling rate and a higher-order integration to further reduce quantization noise.

and by integrator settling error at high sampling frequencies. There is a middle frequency range, where other noise sources are dominant. These noises are reduced by increasing the sampling rate, such that a minimum-noise operating point exists at the high-end of the middle range, just before settling noise becomes dominant. The switched-capacitor topology is better than switched-current in terms of minimum achievable noise, because switched capacitors can reach the thermal noise limit while switched-current circuits are dominated by clock feed-through noise and by distortion. As shown in Fig. 8, second-order continuous-time modulators are limited either by quantization noise (at low sampling frequencies) or by clock jitter (at higher frequencies), and there is no settling-noise range. In order to improve the noise performance of continuous-time circuits, one must either employ higher-order integration or reduce clock jitter. Although the results in Figs. 6–8 were calculated for specific technology parameters, we have found that these observations are valid for a wide range of practical parameter values, where continuous time circuits cannot reach the thermal noise limit.

The total noise power for the circuits discussed above can be computed by taking the RMS value of all noise voltages. In our example, AC97 specifies an input signal of −9 dB and SNR of 80 dB, so we require a circuit with noise power of −89 dB or less. Referring to Fig. 6, this requirement can be met by a second-order switched capacitor circuit with an oversampling ratio in the range 64–362, corresponding to sampling frequency of 3.2–18.1 Mhz. Alternatively, referring to Fig. 8, a fourth-order continuous-time circuit can be used at a low oversampling ratio in the range 16–64 corresponding to a sampling frequency of 0.8–3.2 Mhz. Choosing the continuous time option requires to ensure stability. It is possible to solve the stability problem by using cascade topology, but then the modulator will become sensitive to mismatch between the different stages of the integration. When using a single loop approach, the stability problem can raise a dynamic range problem due to integrator stage gains and input signal scaling. Also, poles of the modulator's transfer function depend on the time constant of the integrators, determined by the product of a resistance and a capacitance. These parameters are not well controlled, and their absolute values may vary among different chips and as a function of temperature, which complicates the design for stability. Clearly, the continuous-time option does not exploit the speed of the CMOS process, and is sensitive to parameter variations. It is preferable to choose the discrete time option with a switched-capacitor circuit, due to the inherent stability of second-order modulators. Also, the transfer function in the SC circuit depends on a ratio of capacitances, which is much better controlled than absolute parameter values. Therefore, it is more immune to process temperature variations. These conclusions confirm and complement the conclusions of Sec. 2.

The above analysis of circuit-level noise shows that switched-capacitor modulator topology has the best noise performance, compared with alternative CMOS circuit topologies. However, oversampling rates must remain much lower than digital circuit clock rates, because of settling noise, limited by analog amplifier gain and bandwidth. It is interesting to note that g_m is the intrinsic limiter of noise performance in a switched capacitor modulator, rather than the sampling capacitor C_s or the oversampling ratio M. This is illustrated in Fig. 9, showing total noise (as in Fig. 6) for various values of C_s while keeping g_m fixed. Increasing C_s leads to a lower usable M while the minimum achievable noise remains constant. This property can be derived with some simplifications as follows: Thermal noise limits the SNR according to Eq. (4), which can be approximated by

$$\mathrm{SNR}^2 \leq V_{PP}^2 \frac{MC_S}{kT} . \tag{13}$$

The settling-noise limited SNR can be approximated from Eq. (5), assuming linear settling and ignoring slew-rate, by an expression of the form

$$\mathrm{SNR} \leq a_1 e^{g_m / f_0 M C_s} . \tag{14}$$

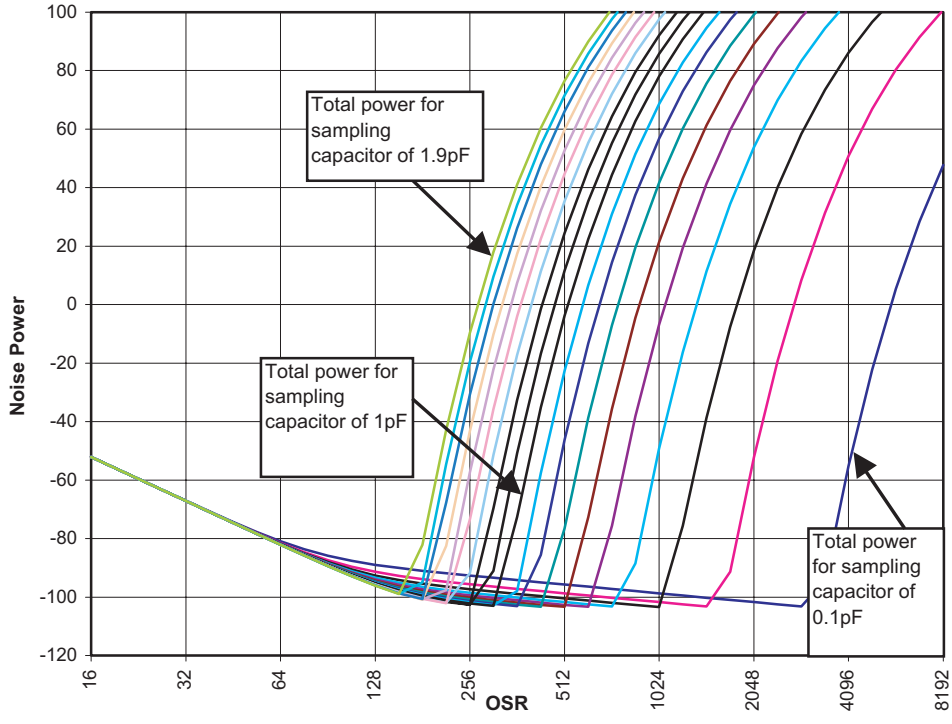

Fig. 9. Total noise power of switched capacitor sigma–delta modulator, for sampling capacitor values from 0.1 pF to 1.9 pF in 0.1 pF steps. The minimum achievable noise power is independent of the selected value of sampling capacitor.

Eliminating MC_s from Eqs. (13) and (14), and assuming that ln(SNR) is approximately constant, we obtain:

$$\mathrm{SNR} \leq a_2 V_{PP} \sqrt{\frac{g_m}{kTf_0}}\,. \tag{15}$$

In advanced processes g_m increases to achieve high speed while the supply voltage drops in order to reduce power dissipation and to protect transistors from high electrical fields. The product $V_{PP}\sqrt{g_m}$ should be kept invariant in order to maintain the SNR performance. In future technology generations, the projected growth of intrinsic g_m is slower than the projected drop of supply voltages. Hence, larger transistors would be required, and the conversion circuits will not gain full benefit of geometrical scaling.

Acknowledgment

The authors would like to express their thanks to Prof. A. Arbel for his valuable comments which helped directing this work.

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