Correspondence

Current Gain of Shallow-Junction Lateral Transistors

A. KOLODNY

Abstract—Two-dimensional current flow in shallow-junction lateral transistors is analyzed. Emitter and base currents in stripe-geometry and circular devices are expressed in terms of a transform of the excess carrier concentration at the base surface. The dependence of current gain on device parameters is presented graphically.

Modeling of lateral transistors is complicated by the two-dimensional nature of current flow in the base. Several authors [1]-[4] have approached the problem by using a simplified model, considering the emitter current to be the sum of one-dimensional components in the lateral and vertical directions. Other authors [5]-[8] have used numerical methods for solving the two-dimensional continuity equation of minority carriers. It has been shown that for many cases the simple quasi-one-dimensional approach is plausible [4], and geometry-dependent factors may be used to relate two-dimensional current to that obtained from a one-dimensional model [6]. However, in the case of very shallow junctions, with depths much smaller than the lateral basewidth, the quasi-one-dimensional methods break down. For such devices (e.g., ion-implanted or mesa-structure devices) the lateral section of the transistor is very small and current flow is purely two-dimensional.

The purpose of this correspondence is to present a simple approximate solution for the two-dimensional dc problem of shallow-junction lateral transistors at low-level injection. Circular devices as well as stripe-geometry devices are considered, while all the above mentioned analyses refer only to stripe-geometry devices. Fig. 1 shows the device structures and defines the notation. Space-charge layer edges are assumed to be at $x = 0$.

Consider first the stripe-geometry p-n-p device (Fig. 1(a)) without a buried layer ($x_{epi} \to \infty$). The excess holes in the base obey the continuity equation

$$\frac{\partial^2 \hat{p}}{\partial x^2} + \frac{\partial^2 \hat{p}}{\partial y^2} - \frac{\hat{p}}{L_p^2} = 0 \tag{1}$$

where $\hat{p}$ is the excess concentration and L_p is the diffusion length for holes. Along the edge of the emitter junction $\hat{p}$ is a constant $\hat{p}_E$ (determined by the junction bias), and along the edge of the collector junction $\hat{p}$ is close to zero. The derivative $\partial\hat{p}/\partial y$ is zero on the x axis due to symmetry, and is taken as zero at $y = y_m$ which is far enough from the emitter. The derivative $\partial\hat{p}/\partial x$ is assumed to be zero at the upper base surface (no surface recombination), and at $x \to \infty$ for a device without a buried layer. By separation of variables the formal solution to (1) is

$$p(x,y) = \sum_{n=0}^{\infty} A_n \exp\{-x[L_p^{-2} + (n\pi/y_m)^2]^{1/2}\} \cdot \cos(n\pi y/y_m) \tag{2}$$

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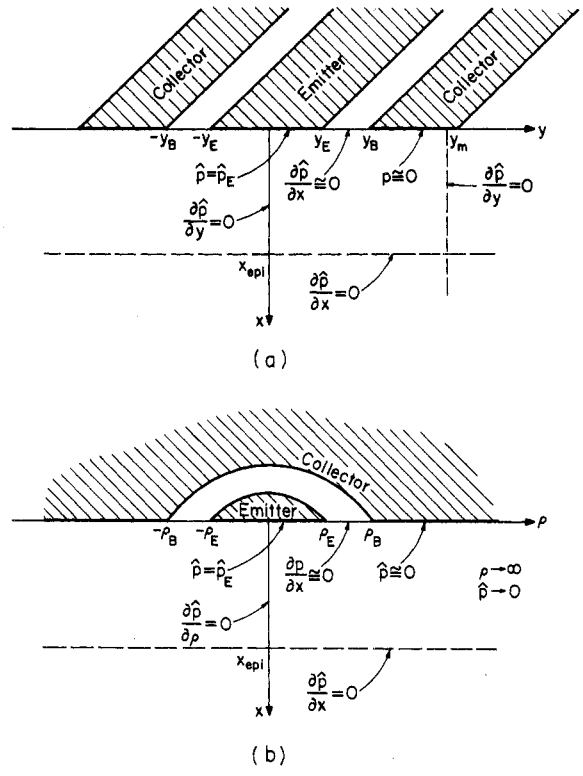

Fig. 1. Schematic view of lateral p-n-p transistors with mesa or very shallow junctions. Boundary conditions for the continuity equation are indicated. (a) Stripe-geometry device. (b) Circular device.

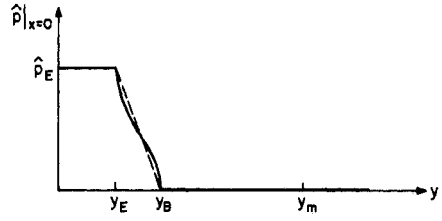

Fig. 2. Excess hole concentration $\hat{p}$ at $x = 0$ (along the junction edges and base surface). The dashed line is a first-order approximation for $\hat{p}$ at the base surface.

where the coefficients A_n must be selected to satisfy the boundary conditions at $x = 0$ (along the junctions and base surface). Since the boundary conditions involve the derivative $\partial\hat{p}/\partial x$ at the base surface, the coefficients cannot be expressed analytically. Simultaneous algebraic equations could be numerically solved for the coefficients [5]-[7], but it is obvious from (2) that they are the cosine Fourier coefficients of $\hat{p}(0,y)$, the excess hole concentration at $x = 0$. $\hat{p}(0,y)$ is unknown only at the base surface ($y_E < y < y_B$), where it may be guessed fairly well (see Fig. 2), and the coefficients may be efficiently obtained by the FFT algorithm.

The calculated coefficients may then be used for evaluating the derivative $\partial\hat{p}/\partial x$ of (2) at the base surface and checking for consistency with the true boundary condition. If the

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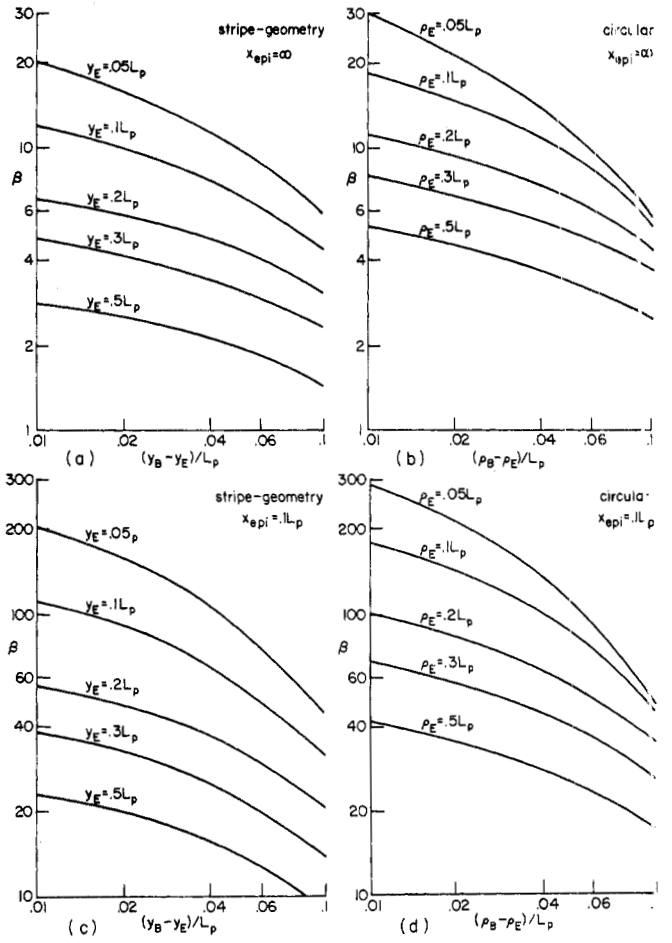

Fig. 3. Calculated current gain versus basewidth for various emitter widths. (a) Stripe geometry without a buried layer. (b) Circular device without a buried layer. (c) Stripe geometry with a buried layer ($x_{epi} = 0.1\ L_p$). (d) Circular device with a buried layer ($x_{epi} = 0.1\ L_p$).

deviation is unacceptable, the guessed hole concentration along the base surface may be corrected according to the sign and magnitude of $(\partial\hat{p}/\partial x)|_{x=0}$, and the process may be repeated iteratively.

The current gain of the device may be calculated from individual currents. The emitter current is

$$I_E = \int_0^{y_E} qD_p \left.\frac{\partial\hat{p}}{\partial x}\right|_{x=0} dy = qD_p \left\{\frac{A_0 y_E}{L_p} + \sum_{n=1}^{\infty} A_n [L_p^{-2} + (n\pi/y_m)^2]^{1/2} \cdot \frac{y_m}{n\pi} \cdot \sin(n\pi y_E/y_m)\right\} \tag{3}$$

which has a strong dependence upon basewidth.

The base current is

$$I_B = \frac{Q_B}{\tau_p} = \frac{q}{\tau_p}\int_0^{\infty}\int_0^{y_m} \hat{p}(x,y)\,dy\,dx = \frac{qL_pA_0y_m}{\tau_p}. \tag{4}$$

Since A_0 is the average value of $\hat{p}(0, y)$, the base current is roughly $qL_p\hat{p}_E \cdot 0.5\ (y_E + y_B)/\tau_p$, using the first-order approximation shown in Fig. 2. The effect of an n^+ buried layer on the device may be represented by introducing the condition $\partial\hat{p}/\partial x = 0$ at $x = x_{epi}$. For such devices, each Fourier coefficient in (3) and (4) should be multiplied by $\tanh\{x_{epi}[L_p^{-2} + (n\pi/y_m)^2]^{1/2}\}$. This boundary condition at $x = x_{epi}$ is not necessarily true if x_{epi} is small. In this case, the hole current penetrating into the buried layer may be comparable to the recombination current in the epitaxial layer [9]. However, the situation may be approximated by taking an effective penetration depth instead of x_{epi}.

For circular devices it is convenient to take $\hat{p} = 0$ as $y \to \infty$. The continuity equation in polar coordinates is

$$\frac{\partial^2\hat{p}}{\partial\rho^2} + \frac{1}{\rho}\frac{\partial\hat{p}}{\partial\rho} + \frac{\partial\hat{p}}{\partial x^2} - \frac{\hat{p}}{L_p^2} = 0 \tag{5}$$

and the boundary conditions are indicated in Fig. 1(b). The formal solution for a device without a buried layer is

$$\hat{p}(x,\rho) = \int_0^{\infty} g(\alpha)\exp[-x(L_p^{-2} + \alpha^2)^{1/2}] \cdot \alpha \cdot J_0(\alpha\rho)\,d\alpha \tag{6}$$

where J_0 is Bessel function of the first kind of order zero, α is a continuous variable, and the function $g(\alpha)$ must be chosen so that the boundary conditions at $x = 0$ are satisfied. In this case, $g(\alpha)$ is the Hankel transform [10] of $\hat{p}(0, \rho)$, defined by

$$g(\alpha) = \int_0^{\infty} \rho \cdot J_0(\alpha\rho) \cdot \hat{p}(0,\rho)\,d\rho. \tag{7}$$

In an analogous fashion, $g(\alpha)$ may be found by applying Hankel's transform to a guess of $\hat{p}(0, \rho)$ and iterating the process if necessary. The current expressions are

$$I_E = \int_0^{\rho_E} qD_p \left.\frac{\partial\hat{p}}{\partial x}\right|_{x=0} \cdot 2\pi\rho d\rho = \int_0^{\rho_E} qD_p \left[\int_0^{\infty} g(\alpha)(L_p^{-2} + \alpha^2)^{1/2} \cdot \alpha \cdot J_0(\alpha\rho)\,d\alpha\right] 2\pi\rho\,d\rho \tag{8}$$

$$I_B = \frac{Q_B}{\tau_p} = \frac{q}{\tau_p}\int_0^{\infty}\left[\int_0^{\infty}\hat{p}(x,\rho)\,dx\right] 2\pi\rho\,d\rho$$

$$= \frac{q}{\tau_p}\int_0^{\infty}\left[\int_0^{\infty} g(\alpha)(L_p^{-2} + \alpha^2)^{-1/2} \cdot \alpha \cdot J_0(\alpha\rho)\,d\alpha\right] 2\pi\rho\,d\rho$$

$$= \frac{q}{\tau_p} 2\pi g(0) L_p. \tag{9}$$

For circular devices with an n^+ buried layer, the function $g(\alpha)$ should be multiplied by $\tanh\{x_{epi}[L_p^{-2} + \alpha^2]^{1/2}\}$ in these expressions.

Calculated current gain β is plotted in Fig. 3 for stripe-geometry and circular devices with various emitter and base-widths. All geometrical values are normalized to units of L_p. For devices with a buried layer $x_{epi} = 0.1\ L_p$ has been used in the calculation. It is evident from Fig. 3 that circular devices are superior to stripe-geometry devices of the same dimensions. The slope of current-gain versus basewidth curves for a fixed emitter width increases with increasing basewidth. This is a consequence of the fact that for narrow basewidths, the base current is almost constant and β varies approximately in proportion to the collector current, while for larger basewidths, the base current starts to increase and enhances the degradation of β. The effect is pronounced in devices with a small emitter.

Measurements have been performed on silicon devices without a buried layer which had shallow ion-implanted junctions, and on indium antimonide devices with mesa junctions oper-

ated at 77 K. The results agree with the above theory within a factor of two, indicating the importance of base-current components other than volume recombination [6], which had been neglected in the model. Application of a quasi-one-dimensional approach [4] to the implanted devices yields values of β which are lower by an order of magnitude than those observed experimentally. For the mesa-structure devices, the quasi-one-dimensional approach cannot be employed at all, since the whole emitter current is injected vertically.

The presented analysis may be employed also for estimating current gains of devices with nonshallow junctions, by assuming that the vertical sidewalls of the emitter contribute a one-dimensional lateral current in addition to the two-dimensional current derived above.

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Silicon p-i-n Photodetectors with Integrated Transistor Amplifiers

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Abstract—**A novel silicon photodetector is presented, incorporating transistor gain in a p-i-n photodiode and its performance is analyzed. Gain and noise power frequency characteristics are analytically derived in terms of an equivalent circuit. These analytical results are in good agreement with experimental results. Noise power is estimated and it is shown that, in the video frequency range, the *S/N* ratio is far superior to that of APD for relatively large signal levels. Detector operational features are described.**

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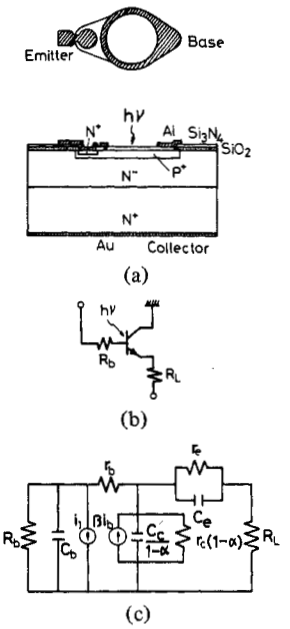

Fig. 1. p-i-n-transistor photodetector. (a) Structure. (b) Fundamental equivalent circuit. (c) Equivalent circuit in a common-collector configuration.

I. INTRODUCTION

Along with rapid advances in optical fiber transmission, optical devices required for these systems have been greatly improved. Optical detectors, such as the p-i-n photodetector [1] and the avalanche photodiode (APD) [2], have been developed mainly for both response speed and low noise. The p-i-n has advantages of easy fabrication and low operating voltage, because of its simple structure compared with the APD. However, as the p-i-n does not possess the same multiplication gain as APD, the p-i-n output performance is limited by the quantum efficiency in the diode depletion layer. On the other hand, phototransistors [3] and photoconductors [3] possessing amplification have insufficient response speed to operate at a bit rate required in the optical transmission systems.

In this correspondence a novel p-i-n photodetector with conventional double-diffused transistor structure (p-i-n transistor) and its characteristics are presented. This p-i-n-transistor photodetector is fabricated in almost the same way as a conventional p-i-n photodiode. Therefore, various inherent advantages of the p-i-n are also valid.

II. STRUCTURE AND CHARACTERISTICS

The p-i-n-transistor photodetector is essentially a double-diffused transistor, as shown in Fig. 1(a). However, there is a much smaller emitter area than the base and a thick depletion layer is provided between base and collector to absorb most of the incident light. Otherwise, the base-to-collector structure is essentially the same as the p-i-n, whose improved properties will be presented elsewhere [1]. A p-i-n with n-type substrate is superior to that with p-type substrate, in relation to response speed, because electron drift velocity is more rapid than hole drift velocity. n^- on n^+ epitaxial wafer (n^-: 110-$\Omega \cdot$ cm resistivity and about 40-μm thickness) was adopted in order that the depletion layer in the n^- collector

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