DESIGN AND MODELLING OF NETWORK ON CHIP INTERCONNECTS USING TRANSMISSION LINES

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ABSTRACT

This paper presents an approach to physical design and modelling of Network-on-Chip Interconnects using on-chip transmission lines. Design guidelines are presented allowing the use of simple models with frequency-independent RLCG parameters. Circuit simulation results demonstrate the validity of this approach in a real design environment.

1. INTRODUCTION

On-chip packet-switched network can potentially become the preferred interconnection approach for future Systems-on-Chip (SoC). Different Network on Chip (NoC) architectures and topologies have been presented in the literature [1, 2, 3, 4]. These on-chip networks provide efficient sharing of global wires, which can be structured so that their electrical properties are optimized and well-controlled.

Global interconnect design in deep sub-micron technologies involves issues such as wire delay, delay variations, crosstalk noise, synchronization, signal integrity and dynamic power consumption [5]. Inductive behavior of the wires becomes important at high operating speeds, but inductance extraction from unconstrained layout is a complicated task, since there is generally no well-defined current return path [6]. Network-on-chip link design should address these issues and simplify their modelling.

We propose the use of on-chip transmission lines (T-lines) [9, 11] as an implementation for NoC interconnects. Dedicated return path enables inductance calculation for T-lines, and well-defined geometry enables easy calculation of their RLC parameters. Optimization of parameterized T-lines for power consumption and wire delay minimization can be easily done. The use of T-lines for critical signals is a common practice in high speed analog design. T-line models used in analog circuits include frequency dependent phenomena such as skin effect and silicon substrate related effects. For large scale digital design it is highly desirable to have simpler T-lines models still suitable for nonlinear transient simulation at the circuit level. A design approach for reducing the frequency dependent phenomena in T-lines behavior is presented in this paper, thus enabling the use of such simple models.

This paper is organized as follows: Section 2 presents general NoC structure and discusses the advantages of implementing NoC links using T-lines. Sections 3 and 4 present a modelling and design approach for NoC T-lines. Section 5 validates the proposed approach by means of circuit simulations. Chapter 6 summarizes the obtained results.

2. GENERAL CONSIDERATIONS

Figure 1 presents an example of a System-on-Chip using a Network-on-Chip. The system resources (computational blocks and memory units) are connected to a mesh of switches interconnected by communication channels. Each channel consists of two fast one-directional point-to-point links. The switches route and buffer messages between the system resources. This communication network is similar to general-purpose computer networks, optimized for the characteristics of monolithic on-chip integration [3, 7, 8]

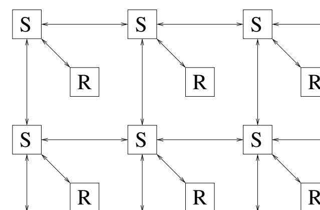

Figure 1: General NoC representation, with switches (S) and resources (R).

The traditional digital VLSI interconnect design approach, which uses wire routing followed by post-layout parameter extraction may not be adequate for NOC interconnections at high frequencies. There is a design closure problem because the electrical behavior of the extracted links deviates from the original design specifications, thus leading to numerous design iterations. It is also highly complex, or even impossible, to extract the inductance of wires unless the current return path is known in advance [11]. It is therefore highly recommended to design the NoC interconnections as transmission lines with their built-in well defined return path and well-defined electrical parameters known a-priori at the early design stages.

We propose to isolate the NoC links from the noisy environment by putting them in dedicated routing channels, thereby avoiding adjacent collinear lines and reducing the number of crossing lines. The Si substrate generally does not provide good return path[12], but, at high frequencies, the capacitance of lines positioned right above the silicon substrate becomes frequency dependent and substrate losses occur, which complicates the modelling. We therefore suggest to shield the NoC lines from below, leading to the previously reported microstrip structure [9, 11] which also benefits from the frequency independent dielectric properties of

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the silicon oxide layer. The remaining frequency dependence of these microstrip T-lines is only due to the skin effect.

3. NOC DESIGN AND MODELLING APPROACH

Figure 2 presents the cross-section of microstrip transmission line topologies which include a signal line(s) accompanied by ground return path(s). These microstrip geometries meet the closed environment condition [11], whereby the shielding provides this return path and also eliminates the coupling to the conductive silicon substrate and to other wires. Consequently the crosstalk is kept low and the line impedance is well controlled. This shielding methodology also reduces the inductance of the T-line structure, thereby reducing overshoots and ringing noise. The presented T-line structure allows side shielding of the signal line, as shown in Figure 2(b).

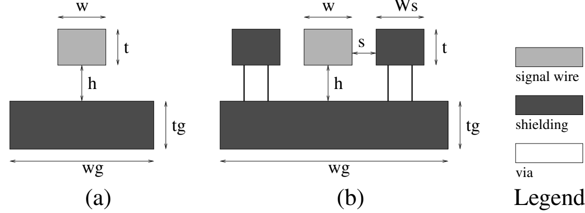

Figure 2: Cross-section of single transmission line in a microstrip geometry.

A general simulation model for the presented T-line topologies is shown on Figure 3. The model consists of a multisegment RLCG network, which describes the T-line behavior by means of R,L,C,G per unit length. At list 10 repeated segments are practically used per one on-chip wavelength at the bandwidth higher end frequency for obtaining the acceptable waveform accuracy. The frequency dependent effects can be described by using appropriate RLC filter networks, such as ladder circuits[12]. This model [12] was verified by VNA measurements up to 110 GHz. In this paper we use this model as our reference model and denote it by R(f)L(f)C(f).

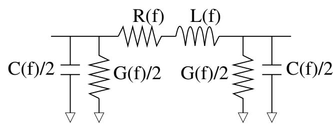

Figure 3: General frequency dependent RLCG representation of a transmission line.

Figure 4 presents a RC T-line model compared with the full R(f)L(f)C(f) model (simulation setup are given in section 5. It can be seen that inductance affects delay, transition rates, and causes signal overshoots. Figure 4 clearly demonstrates that it is necessary to include the inductance parameter into the T-line model.

It is important to notice, that in these microstrip structures only R and L parameters change with frequency due to skin effect [12]. General physical behavior of R and L parameters of T-lines (due to skin effect) is given in Figure 5. At low frequencies, the current distribution in the metal lines is uniform, namely the resistance of

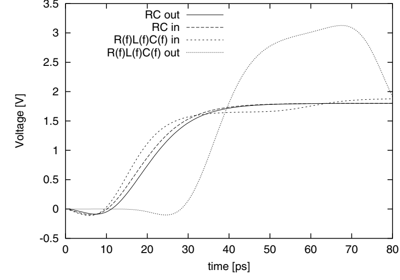

Figure 4: RLC(f) and RC T-line models, near end and far end, t=4μ, tg=1.25μ.

the T-line is the Ohmic DC resistance (signal line + return path metals), and the inductance per unit length is the low frequency limit inductance, for which the expressions were developed and reported in [10]. At the high frequencies, the inductance reaches the high frequency limit inductance L_∞. The resistance does not saturate, but approaches an asymptotic $\sqrt{f}$ behavior at high frequencies. These parameter variations with frequency are significant, and might have non-negligible effects on waveforms of fast digital signals. Our methodology advocates to reduce skin-effect

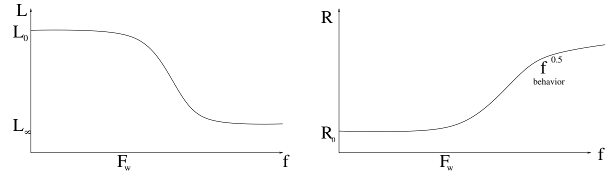

Figure 5: Physical behavior of R and L parameters.

and the resulting frequency dependence. To provide this, the skin depth has to be calculated at maximal operation frequency and the T-line's thickness is designed to be smaller or equal to the calculated value of the skin depth. The skin depth calculation is presented in (1) and the condition keeping the frequency dependent phenomena low is presented in (2).

$$\delta(f) = \sqrt{\frac{2}{\pi \cdot f \cdot \mu \cdot \sigma}} \quad (1)$$

$$t \leq \delta(f) \quad (2)$$

The constraint (2) leads to close to uniform current distribution in the wire. Another condition gives the width of the bottom shield which in the structure of Figure 2(a) equals to:

$$w_g = w + 2 \cdot (t + h) \quad (3)$$

A smaller width may violate the closed environment condition, whereas a larger width may cause lateral skin effect. Under these constraints, other transmission line parameters (such as width and dielectric thickness) can be varied to achieve the desired T-line characteristics. In practical situations, it is not always possible to meet condition (3) in the given technology metal stack. Hence, we need a simple model which provides a good approximation for the frequency dependence effects.

4. PROPOSED SIMPLE MODEL FOR T-LINE

A simple model for T-line topologies can be seen on Figure 6. This model consists of multisegment RLC network where the R,L,C parameters are frequency independent. The main challenge in T-line modelling is therefore to determine the network parameters. There are several possibilities to do this: T-line inductance can be presented by L_0 or L_∞, and the resistance can be presented by R_0 or the resistance at a selected high frequency denoted by R_{HF}. Following this approach, four models could be presented:

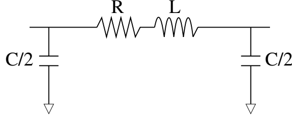

Figure 6: General frequency indepenent RLC representation of one of N segments of a microstrip transmission line.

$\underline{R_0L_0C}$ - represents a T-line model where the line resistance and inductance are described by DC resistance and low frequency inductance respectively. Low frequency inductance can be calculated from [10]. R_0 calculation is presented in (4).

$$R_0 = R_0(signal) + R_0(ground) =$$

$$= R_\square(signal) \cdot \frac{1}{W_s} + R_\square(ground) \cdot \frac{1}{W_g} \qquad (4)$$

Where $R_\square(signal)$ and $R_\square(ground)$ are the sheet resistance of signal and ground line metals respectively, W_s and W_g are the width of signal and ground line respectively.

$\underline{R_0L_\infty C}$ - represents a T-line model where the line resistance is described by DC resistance and line inductance is described by its high frequency limit. High frequency inductance can be calculated from (5).

$$L_\infty = \frac{\tau_{of}^2}{C}; \tau_{of} = \frac{l \cdot \sqrt{\varepsilon}}{c_0} \qquad (5)$$

Where τ_{of} is time of flight and C is T-line capacitance which can be calculated, for example, from [13]. l is the T-line length, ε is the dielectric constant and c_0 is the speed of light.

$\underline{R_{HF}L_0C}$ - represents a T-line model where the line resistance is described by the high frequency resistance given at frequency f_1, and line inductance is described by LF inductance. A suggested value for the frequency f_1 is the higher end of the on-chip signal bandwidth $0.5/t_{rise}$.

$$R_{HF} = R(f_1) = R(f_1)_{signal} + R(f_1)_{ground} =$$

$$= R_\square(signal) \cdot \frac{1}{W_s} \cdot \frac{t_{signal}}{\delta(f_1)} + R_\square(ground) \cdot \frac{1}{W_g} \cdot \frac{t_{ground}}{\delta(f_1)} \quad (6)$$

$\delta(f = f1)$ is the skin depth at frequency f1 and can be calculated from (1).

$\underline{R_{HF}L_\infty C}$ - represents a T-line model where the line resistance is described by high frequency resistance and line inductance is described by its high frequency limit.

All the models as well as the reference model can be generalized to differential T-line structure, not discussed in this paper.

5. COMPARISON BETWEEN THE DIFFERENT SUGGESTED MODELS

In order to decide which of the T-line models is most appropriate, circuit simulations were performed on four models and the waveforms were compared to the reference model.

The simulation setup which includes the proposed models along with the reference model is presented on Figure 7. This setup for

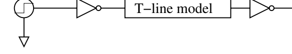

Figure 7: Simulation setup.

each transmission line consists of pulse generator, driver, T-line and receiver. The pulse generator gives waveform with transition time of 10psec; this waveform is fed into the driver. The driver is a CMOS inverter (in a 0.18μ CMOS technology) designed to be sufficiently large in order to drive the T-line (about 20 psec transition time at the T-line input). The receiver is a minimal size inverter. The waveforms at the far end of each transmission line were compared to the reference model.

Two sets of simulations were performed, one with a thick line: t=4μ and tg=1.25μ, and another with a thin line: t=1.25μ and tg=0.3μ. The lines length is 3mm in both cases. Figure 8(a) and 8(b) present the full R(f)L(f)C(f) model along with two simple models: R_0L_0C and $R_0L_\infty C$. It can be seen that in these specific cases L_∞ gives more accurate approximation than L_0 by means of propagation delay and slow rates. The difference in propagation delay (at 50% output) between the two simple models is equal to 3.5ps. The total propagation delay from the near end to the far end of the T-line is equal to 23.7psec which is nearby the same as the time of flight according to (5). This means that the difference in the propagation delay is 15% of the total propagation delay across the line in this specific case. The remaining parameter to be determined in the simple T-line model is the resistance parameter which can be presented by R_0 or R_{HF}. This parameter depends on the condition (2). Figure 9(a) and 9(b) show the results for the thick line and for the thin line respectively. It can be seen that in both cases (t=4μ, tg=1.25μ and t=1.25μ, tg=0.3μ) R_0 gives better approximation for the T-line resistance. The bandwidth of an on-chip repetitive signal spans between the inverse of the signal period till the inverse of the transition times, thereby

$$\frac{1}{T} < BW < \frac{0.5}{t_{rise}} \qquad (7)$$

We therefore have to examine the frequency dependence of the model in this given bandwidth. In our case, 1/T=1 GHz and the inverse of the transition times may be as high as 25 GHz. At 25 GHz, the skin depth of Al and Cu is 0.6μ and 0.45μ respectively. Both T-line thicknesses which we have used in this example therefore give rise to some frequency dependence, as expected by 2. In the figures we can see that the more thick line is more frequency dependent as expected.

6. SUMMARY

An approach for the design and modelling of NoC links using T-lines was presented. At high speed RC modelling of the wires is insufficient and we have to consider the line inductance as well

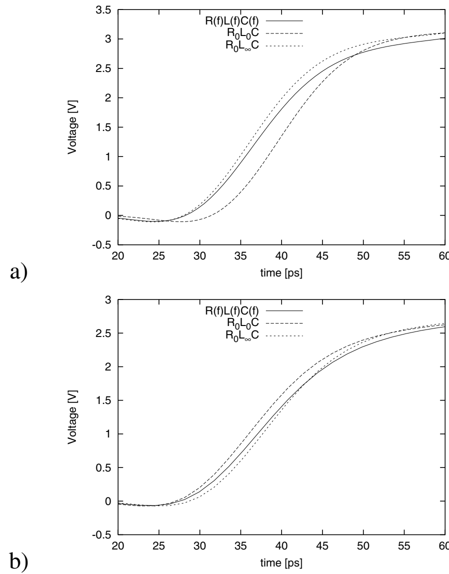

Figure 8: R(f)L(f)C(f), R_0L_0C, $R_0L_\infty C$; for a) t=4μ, t_g=1.25μ and b) t=1.25μ, t_g=0.3μ.

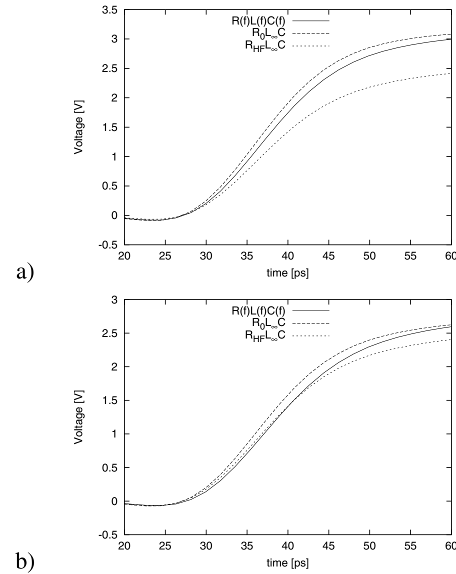

Figure 9: R(f)L(f)C(f), $R_0L_\infty C$, $R_{HF}L_\infty C$; for a) t=4μ, t_g=1.25μ and b) t=1.25μ, t_g=0.3μ.

as the skin effect. A criterion was determined for minimizing the frequency dependence of the model parameters. Four simple T-line models were presented and compared with a reference model which includes the full skin and proximity effects. In the studied practical examples the most appropriate approximation was found to be the one which uses the DC resistance and the high frequency limit inductance, which is also the simplest model to compute.

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